Master's Thesis

Research on Efficiency-Optimized Design Methodology of Semi-DAB Converters for Battery Charging Applications

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Advisor
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3 July. 2020

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Abstract

The semi-dual-active-bridge (semi-DAB) is a topology that advanced converter derived from a dual-active-bridge (DAB) converter. The DAB is an outstanding converter topology of DC-DC converters for battery charging applications, since the DAB converter has many advantages such as being capable of high-power, having a high power density, and being insulated by a high-frequency transformer for safety and reliability. However, since the H-bridge connected to the battery is composed of switches, there is a risk of shoot-through when switching modulation faults occur. Therefore, the topologies of the semi-DAB converter, which can prevent the shoot-through fault by replacing the high- or low-side switches with the diodes, have been studied and proposed. Typically, in the design of voltage gain for the semi-DAB, it is almost set to one to minimize the rms current and the current stress of the converter. However, in the battery charging dc-dc converter, the input voltage is much higher than the output voltage for fast charging speed. Therefore, in such charging applications, it is not always possible to design the unity voltage gain to improve the power conversion efficiency of the converter.

This thesis proposes a design methodology to increase the efficiency by reducing the conduction loss in the semi-DAB, which can be obtained by charging the voltage gain. First, through the loss analysis of semi-DAB, the main cause of loss reduction in semi-DAB is discussed. Then, after the basic operation principle and waveform of the semi-DAB in SPS (single-phase-shift) are presented, a mathematical analysis is derived for the basic current and power expression related to voltage gain of the semi-DAB.

Mostly the voltage gain is designed as 1 because the waveform of the current on the primary side of the converter must be flat to reduce the loss by reducing the RMS current. But, in most cases of charging applications, the voltage on the secondary is lower than that of the primary side, so the current on the secondary side is much greater than that of the primary side. So, the current on the secondary side, which accounts for a dominant portion of the semi-DAB converter loss, can be obtained by multiplying the current on the primary side by the voltage gain. Therefore, it is intended to optimize the voltage gain that has the lowest conduction loss by considering both the primary side RMS current and the voltage gain. And the proposed method is mathematically analyzed to derive the optimal voltage gain that can improve the efficiency by minimizing the conduction loss of the semi-DAB. The reliabilities of the proposed design method is verified through the simulations using PSIM circuit simulation software. In addition, a 1.5-kW semi-DAB converter prototype is developed for experiments to verify the validity of the proposed method.

Additional advanced modulation is also applied to the proposed converter to improve the efficiency under various load conditions. In particular, an EPS (extended-phase-shift) modulation is applied to the semi-DAB, which can reduce the circulating power, reactive power, of the converter. Thus, by applying EPS, an increasing on the efficiency of the semi-DAB converter can be expected. So, the voltage gain

design method can improve problems that are not best for all loads condition through EPS. Therefore, it is required to change the basic SPS modulation to EPS modulation to verify the feasibility of improving efficiency in the various load situations at the optimized voltage gain values in the previous chapter. It is also verified by simulation and experiment with the 1.5-kW prototype semi-DAB converter.

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List of Abbreviations

DC	Direct Current
EV	Electric Vehicle
OBC	On-board-charger
DAB	Dual-Active-Bridge
Semi-DAB	Semi-Dual-Active-Bridge
G2V	Ground-to-Vehicle
SPS	Single Phase Shift
EPS	Extended Phase Shift
DSP	Digital Signal Processor
PWM	Pulse Width Modulation
ZVS	Zero Voltage Switching

I. INTRODUCTION

In recent years, interest and research on DC-grid have been spreading greatly as large-capacity direct current (DC) loads such as ESS (Energy storage system) and internet data center (IDC) and DC generation facilities of renewable electrical energy sources such as Photovoltaics (PVs), fuel cells and wind power generators have increased. And the rapid increase in the number of electric vehicles (EVs) due to environmental regulations in each country also raises the need for DC distribution. DC distribution system is suitable for renewable energy and future DC digital load. It has more simple power conversion process than existing alternating current (AC) distribution system, so DC distribution can supply high-quality and high-efficiency power [1]-[4]. The circuit diagram between DC-grid and DC-loads are shown as Fig. 1.1. A DC grid is formed through AC/DC conversion from the AC grid, and several DC loads are connected to the formed DC grid. When DC loads are connected to a DC distribution, there is no reduction in power quality due to variation in the load compared to AC distribution.

Globally, Electric Vehicles have emerged as an alternative to environmental regulations to save energy and reduce greenhouse gas emissions, making efforts to develop technologies and expand markets. Therefore, demand for EV is rapidly increasing every year. As a result, many studies have been conducted on infrastructure technologies related to EVs [5]-[7]. The development of electric vehicles is increasing the capacity and voltage of the battery to increase the all-electric-range (AER). For high-speed charging, the input voltage of the charging station getting much higher, and the power capacity of the charging converter is also being increase from several kW to tens of kW.

The charging methods of electric vehicles are largely divided into AC and DC charging. In case of AC charging method, the battery is charged after rectifying to DC voltage through on-board-charger

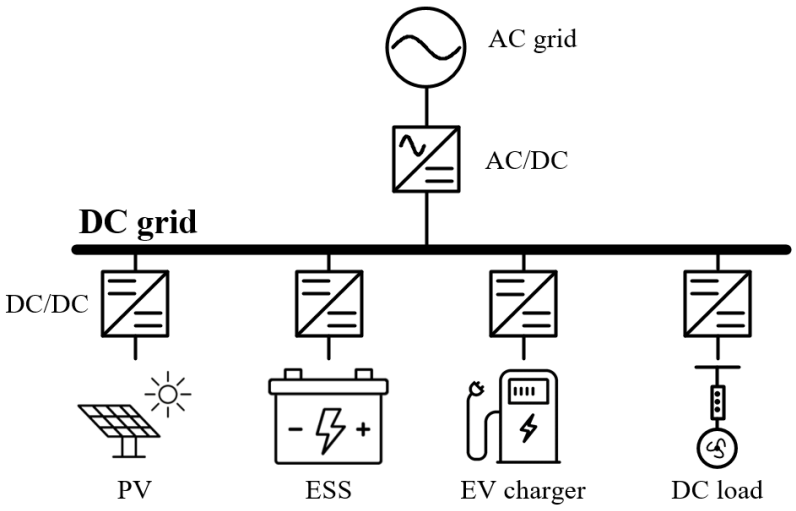


Fig. 1.1 DC-grid with various DC generator and DC loads in circuit diagram

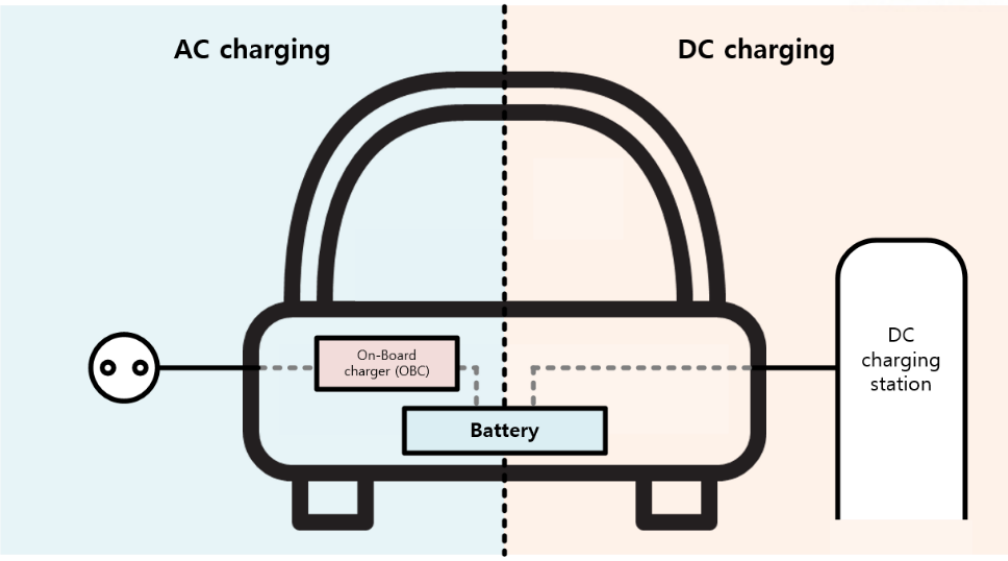


Fig. 1.2 Difference charging process between AC and DC charging for Electrical Vehicle (EV)

(OBC) in EV. Therefore, AC charging performance is limited by the specifications of the OBC already installed inside the vehicle. Because OBC has a fixed power capacity and voltage range because of the protection function, so it is impossible to charge the battery more than a certain amount of power capacity or high-speed. However, In the case of DC charging, the DC charger is directly connected to the battery in EV. Therefore, rapid charging of EV is possible because DC charging converters can be provided with a large amount of power capacity and high voltage. Fig. 1.2 visually shows the difference charging process between AC charging and DC charging in EV. Figure 1.2 shows that AC charging charges the battery through OBC, and DC charging charges the battery directly. Therefore, DC charging is much more advantageous for fast charging for EVs.

In charging applications, concerns about battery accidents and safety issues are also growing as the EV battery charge capacity and voltage are growing. Among the battery accidents, short circuit accidents are the most dangerous because they can cause large-scale fires, and they occur the most frequently among battery accidents [8]. Referred to incidents in the last five years on the EV, approximately 52% were caused by internal short circuit (ISC), and about 26% were caused by external short circuit (ESC) [9]. ISC refers to a short circuit phenomenon in the battery caused by a chemical reactions or foreign substances. ESC means a short circuit caused by external circuit outside the battery. Therefore, in order to increase the safety and reliability regarding the EV battery it is advantageous when using the circuit for preventing the short circuit accidents of the battery.

The dual-active-bridge (DAB) converter is outstanding candidate topology of DC-DC converters for charging batteries of EV [10]. Because the DAB converter can handle large-capacity power, and have a high power density due to the high frequency transformer, and have good safety and reliability due to isolation through the transformer [11]-[12]. In addition, bidirectional power conversion is possible, and

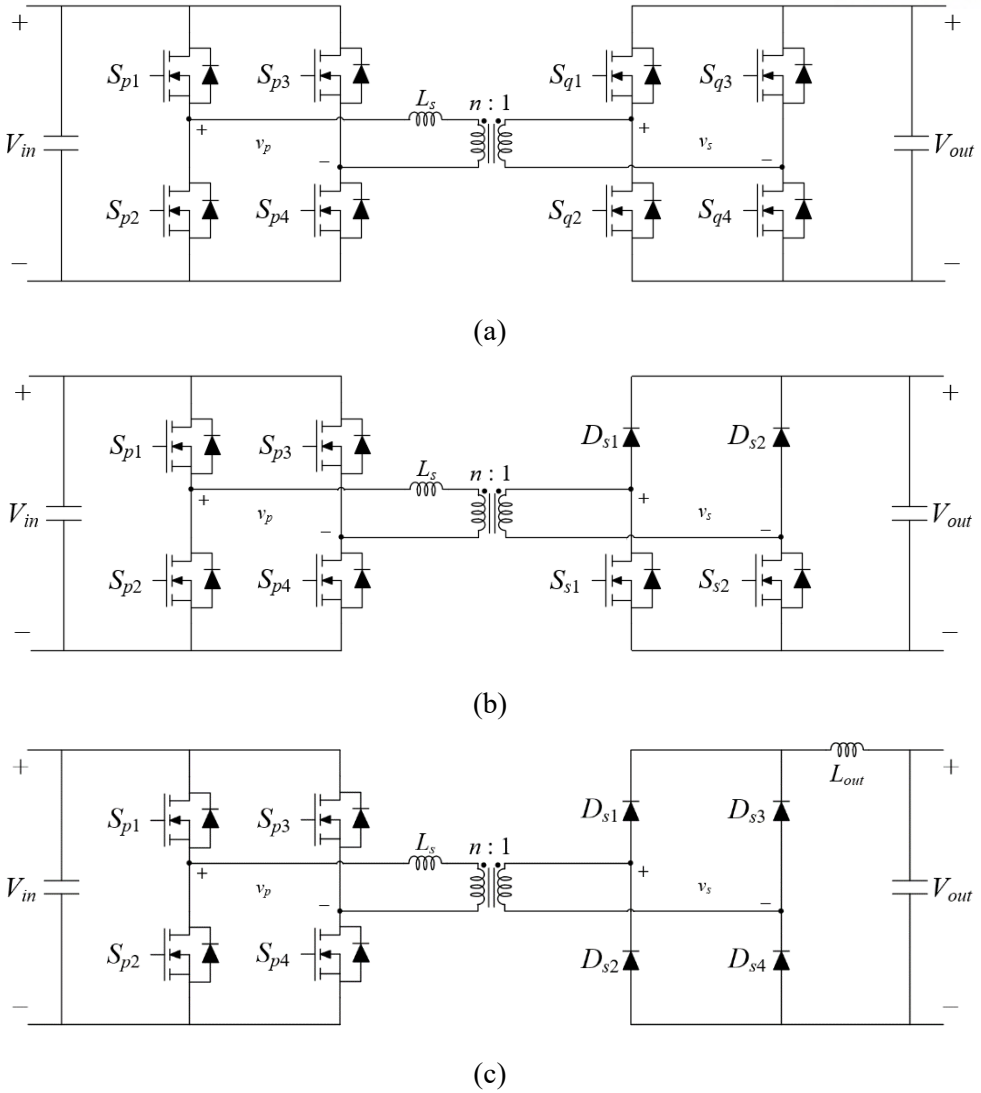


Fig. 1.3 Circuit diagram of (a) Dual-active-bridge (DAB), (b) Semi-dual-active-bridge(semi-DAB) and (c) full-bridge dc-dc converters.

even if the voltage level between the two ports is different, it can be handled by turn ratio and the control of switching. On the other hand, in the battery application of DAB, it has disadvantageous in terms of safety because it has some possibilities of occurring shoot-through [13]-[14]. Because, in most switch failure situations, the MOSFET fails short-state [15]. The short-circuit fault situation of the switch is caused by overvoltage applied to the MOSFET, excessive temperature rise, or internal failure of the switch [16]. This fault cause can often occur due to design failure or insufficient margin of the converter. And short-failure accidents are more dangerous than open-failure and difficult to deal with because diagnosis time must be much shorter. Therefore, if the circuit itself can prevent a shoot-through situation of the converter, no additional device is required to diagnosis short-failure and prevent it. This is why semi-DAB converters, which can prevent shoot-through situations on circuitry way, have advantages over the conventional DAB converters. Thus, the topology that complements these disadvantages of

DAB is semi-DAB.

The semi-dual-active-bridge (semi-DAB) is the topology that replaces two switches located in the upper leg of a secondary port in the DAB with two diodes. Fig. 1.3 shows the circuit diagrams of DAB, semi-DAB and full-bridge dc-dc converter. It has a similar circuit structure, but there are differences in the secondary side circuit. All these converters are isolation converter, even if there is a fault situation on the primary side, the isolation of the transformer can reduce the effect on the secondary side battery.

Since the loss of the switch is relatively smaller than the diode loss, the efficiency of the semi-DAB is lower than that of the DAB. But the topology of semi-DAB converter can prevent the shoot-through issue due to a switch fault, and increase reliability compared to DAB. And even if the fault situation of the secondary side switch occurs, it can prevent the circuit from short-circuit. The semi-DAB converter is not capable of bidirectional power conversion, but bidirectional power conversion is not required in G2V (ground-to-vehicle) applications such as EV charging. And since the two switches in the secondary side lower leg are still active devices, multiple modulation techniques or additional control are possible.

And the full-bridge DC-DC converter consists of four diodes in the secondary side shown as Fig. 1.3 (c). It is compared to semi-DAB, secondary side consists of 4 diodes. In the secondary-side voltage of the semi-DAB generating a zero voltage interval, however, the secondary voltage waveform of the full-bridge dc-dc converter does not generate a zero voltage interval [17]-[19]. Therefore, the switches on the secondary-side of the semi-DAB can operate with zero-voltage-switching (ZVS). So, the turn-on loss can be neglected in the secondary switches in semi-DAB compared to the full-bridge dc-dc converters. And also, the full-bridge dc-dc converter has the disadvantage that the secondary side voltage spike is large due to the ringing between the junction capacitance of the secondary diodes and the leakage inductance of the transformer. Therefore, since the filter inductor must be additionally attached to the output port, so efficiency and power density of the full-bridge dc-dc converter are lower than the semi-DAB converter [20]. The semi-DAB converter was first presented in [21], with symmetrical dual-pulse width modulation (PWM) and phase shifted control was proposed. Since then, studies on the ZVS range expansion, and various modulations about the semi-DAB converter have been published and are still actively being studied [22]-[24].

This thesis introduces the semi-DAB and proposes a voltage gain design methodology of semi-DAB to optimize efficiency in battery charging applications. In particular, a voltage gain method that minimizes the conduction loss of the secondary side connected to the battery is analyzed and proposed. Also, by applying additional modulation, the proposed method shows the feasibility to further maximize the efficiency. The details of the theses are organized as follows: Section II presents theoretical analysis and operational principles of the basic topology for semi-DAB, and introduces the voltage and current waveforms for each operational principle. Also, through the power loss analysis of semi-DAB, which element is the main loss in semi-DAB. In Section III, the concept and theory of the proposed voltage gain methodology for efficiency optimization of semi-DAB is introduced. The proposed gain design

also modifies the gain value to minimize the conduction loss by the equation. And the validity of the proposed gain design method is verified through simulation with MATLAB and PSIM. Finally, the final verification is performed with a hardware experiment. Section IV verifies the feasibility of the advanced modulation method applied to semi-DAB. It introduced the concept of the extended phase shift (EPS), and explains the differences between the existing single phase shift (SPS). And the validity of the additional modulation applications are verified using PSIM simulation and through the experimental results. Through this section, the feasibility can be confirmed that additional modulation can provide additional efficiency improvements. And the thesis concludes proposal in the last section.

II. Analysis of Semi-Dual-Active-Bridge(Semi-DAB) Converter

The semi-dual-active-bridge (Semi-DAB) converter is one of the unidirectional isolated DC-DC converters. In this chapter, the basic topology and operational principle of the semi-DAB are described, and the numerical expressions for basic power and current are derived. And it also shows the major loss factor through the power loss analysis of the semi-DAB.

2.1 Theoretical Analysis and Operational Principles

Fig. 2.1 shows the circuit schematic of semi-DAB. The semi-DAB consists of full-bridge in primary and secondary side which are replaced the upper leg switches of full-bridge into the diodes. And primary and secondary side are connected by high-frequency transformer that also can have function of galvanic isolation. The leakage inductance of the transformer determines the amount of power that the semi-DAB can handle. It can be used as leakage inductance that exists in the transformer itself, but it can be designed according to the amount of available power and used externally. The magnetizing inductance of the transformers also exists, but because it has relatively large inductance value, the impedance of magnetizing inductance is large and is not considered as an open circuit. Therefore, the leakage inductance of the semi-DAB can be implemented by designing the value of the external leakage inductance according to the desired power. The primary side H-bridge consists of four switches S_{p1} – S_{P4}, and the secondary side semi active bridge includes of two diodes D_{s1}, D_{s2}, and two switches S_{s1}, S_{s2}. And the turn ratio of the transformer connecting the bridges on both sides is defined as $\frac{1}{n}$ (n:1). The series inductor that determines the available power is represented by L_s, and is the sum of the actual leakage inductance of the transformer and the external inductance designed.

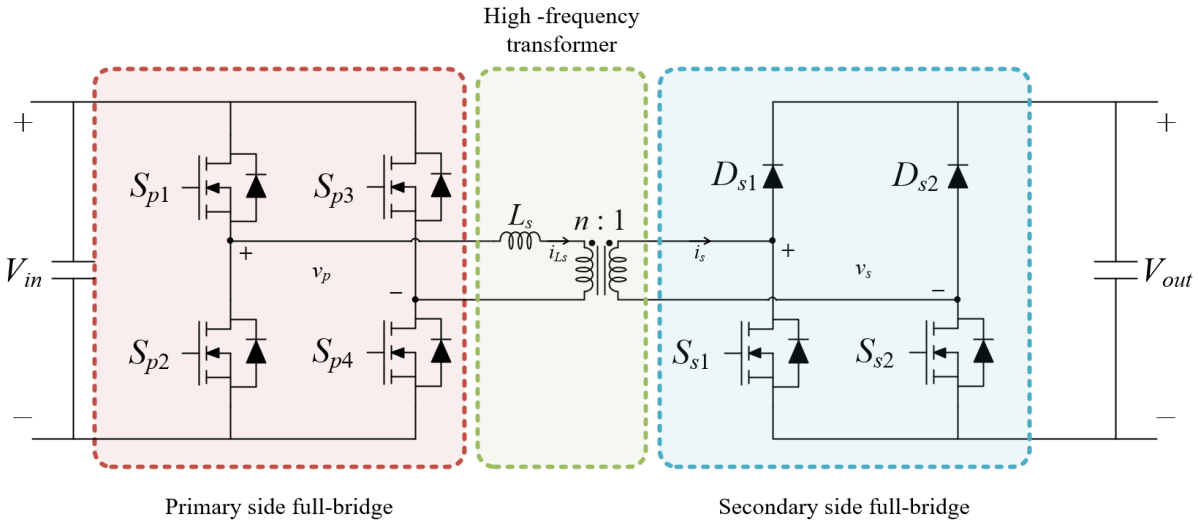


Fig. 2.1 Circuit topology of Semi-DAB

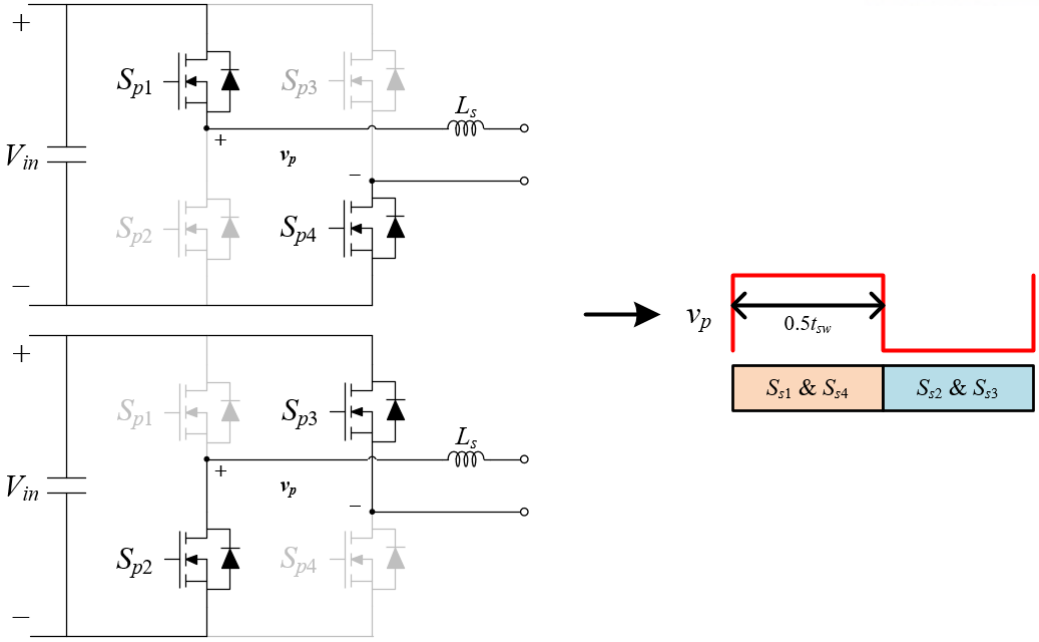


Fig. 2.2 Basic switching principles and voltage waveform of SPS having a 50% duty

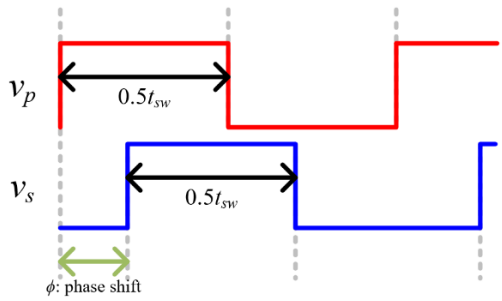


Fig. 2.3 Conceptual diagram of SPS modulation in DAB

The switches in primary side and secondary side are driven by 50% duty cycle of square waveforms, which called single-phase-shift (SPS). SPS is the most basic phase shift modulation, the main advantage is that it is possible to simply convert power [25]. Fig 2.2 shows the switching principle and the voltage waveform of the SPS with 50% duty, where the v_p is the primary transformer voltage. As shown in Fig 2.2, In SPS modulation, the two switches located diagonally are switched on and off simultaneously and operate complementarily. The two switches located diagonally (S_{p1}–S_{p4}, S_{p2}–S_{p3}) always operate in pairs. As depicted in Fig 2.3, the primary and secondary side have fixed 50% duty cycle of square waveforms. The v_p shown in Fig. 2.3 represents the primary transformer voltage, and v_s represents the secondary transformer voltage. The power conversion is controlled according to the phase shift angle ϕ between the rising edges made by the primary side and secondary side voltages which are v_p and v_p. The circuit structure and switching principle on the primary side are the same as DAB and semi-DAB, but there are some differences on the secondary side.

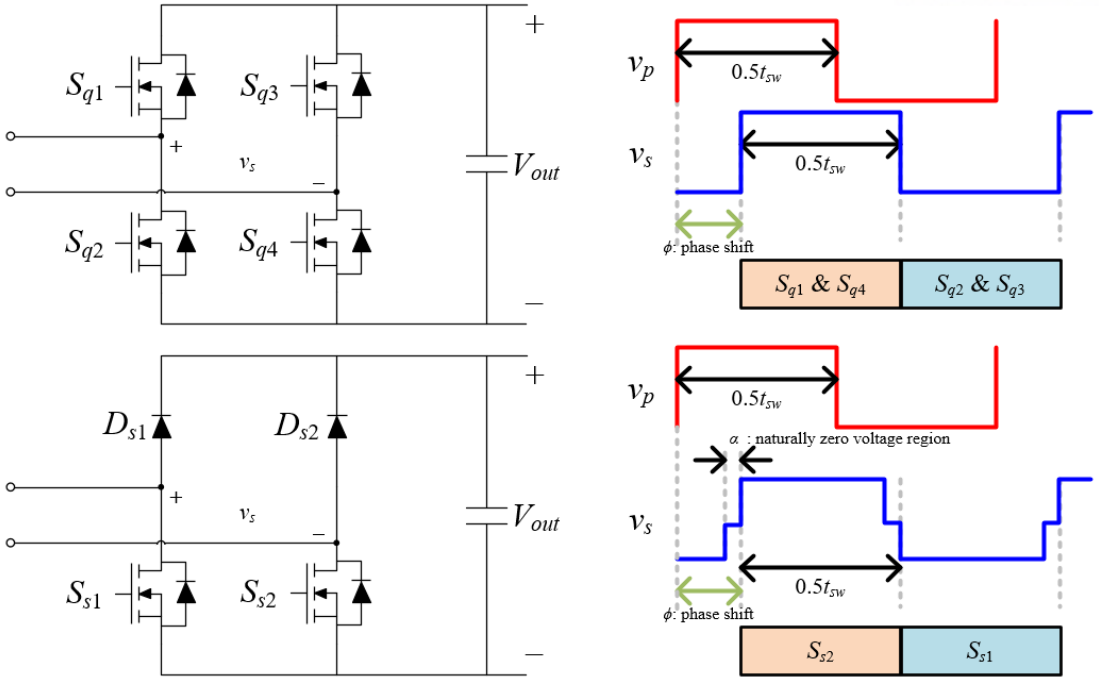


Fig. 2.4 The difference of the switching modulation and voltage waveform in secondary-side between the DAB and semi-DAB when SPS modulation

The SPS switching operation in DAB and the SPS switching operation in semi-DAB are depicted in Fig. 2.4. The secondary-side switching operation of the SPS modulation in the DAB is the same as the primary side switching operational principle. The two switches of secondary-side located diagonally are switched on and off simultaneously and operate complementarily. The two switches located diagonally (S_{q1}–S_{q4}, S_{q2}–S_{q3}) always operate in pairs. This switching operation forms a 50% duty square waveform, as same with primary-side. However, for semi-DAB, S_{q1} and S_{q2} in DAB are replaced by diodes D_{s1} and D_{s2}, so that only the switches S_{s1} and S_{s2} located in the lower leg in secondary-side can be controlled. In semi-DAB, S_{s2} turn on which is existing in the same position in S_{q1} and S_{q4} of DAB. In the meantime, S_{s1} has been turned off because it operates complementary to S_{s2}. The difference from semi-DAB to DAB is shown in the voltage waveform of the secondary-side. There is an interval in which the voltage of the secondary-side becomes zero, which is a characteristic that results from the switch where the current can flow in both directions being replaced by a diode that has unidirectionality. As a result, the phase shift of the primary and secondary sides of the semi-DAB changes the effective voltage applied to the series inductor L_s, controlling a waveform of current.

The semi-DAB converter can be simplified by the model that the two H-bridges connected by the power series inductance, which is shown as Fig. 2.5. This is equivalent circuit of semi-DAB which includes transformer. This equivalent circuit denotes that the waveform of the semi-DAB is greatly affected by the voltage ratio m, $m = nV_{out}/V_{in}$ where n is the turns ratio of the transformer. In particular, charging

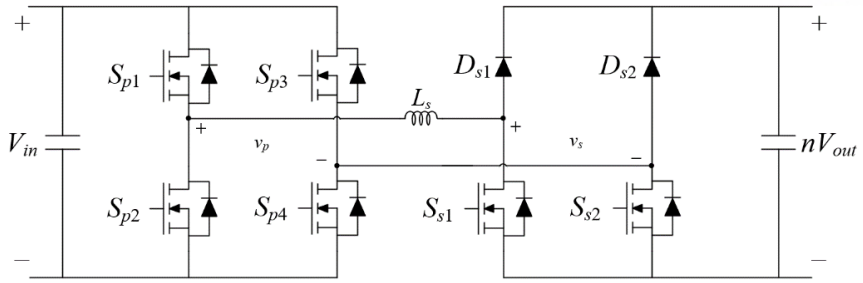


Fig. 2.5 The simplified model that the two H-bridges connected by the series inductance of semi-DAB

application covered in this thesis, the voltage gain of the transformer has a large effect on the waveform because the voltage difference between the input and the output side is significantly large.

The operating voltage and current waveforms of the semi-DAB converter with varying voltage gain can be illustrated as depicted in Fig. 2.6. As the voltage gain varies based on 1, it can be seen that the current waveform is also changed. When m=1 (Fig. 2.6(b)), the input voltage V_{in} equal to the product of the output voltage and the turn ratio, nV_{out}. This create intervals in which the voltage difference is zero across the inductor, resulting in a flat current waveform compared to m<1 (Fig. 2.6(a)) or m>1 (Fig. 2.6(c)). The current waveform is inclined, the peak current and rms current become large. The voltage gain m is defined as (1),

$$m = \frac{nV_{out}}{V_{in}} \tag{1}$$

where n is turn ratio of transformer.

The operating of the semi-DAB is composed of six intervals, as shown in Fig. 2.6. The half-cycle of operating is the same as the negative direction of the other half-cycle. In each section, the current of leakage inductance i_{Ls} is given by

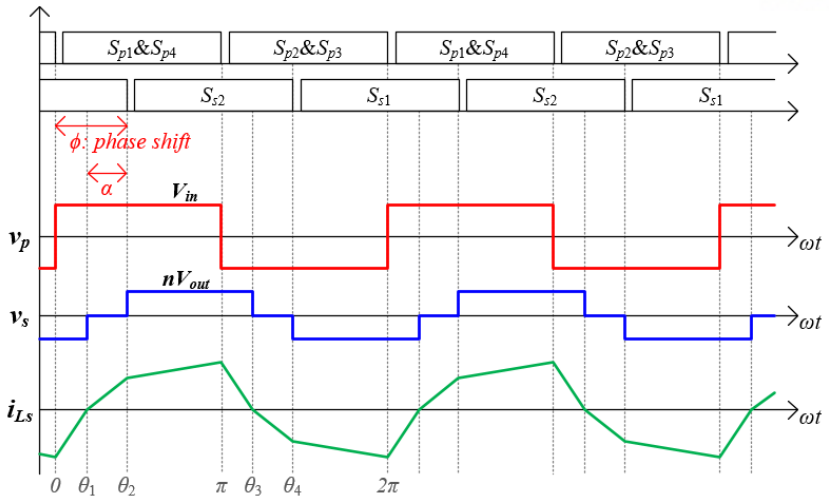
$$i_{Ls}(\theta) = \frac{v_p(\theta) - v_s(\theta)}{wLs}(\theta - \theta_s) + i_{Ls}(\theta_s), \quad for\ \theta_s < \theta < \theta_f \tag{2}$$

where the L_s is the leakage inductance and the ω is the switching frequency in radian/sec.

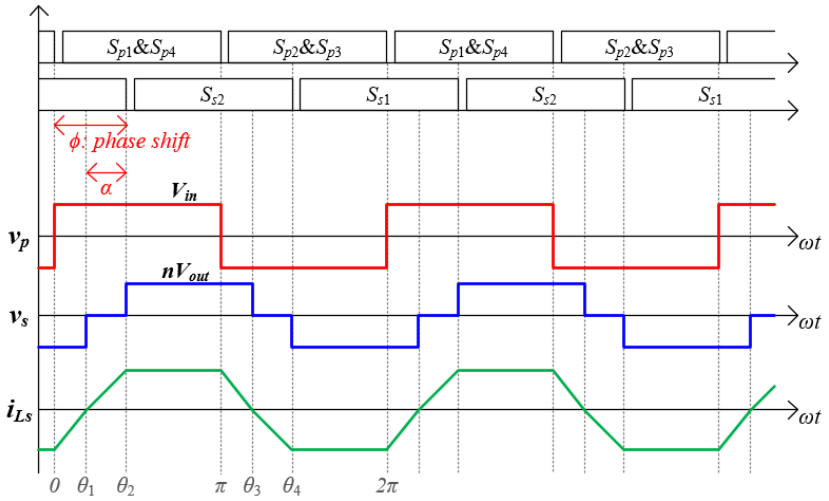
In interval 1 between $0 < \theta < \theta_1$ (ϕ–α), $v_p(\theta) = V_{in}$ and $v_s(\theta) = -nV_{out}$. So, the current in interval 1 is given in the equation (3),

$$i_{Ls}(\theta) = \frac{V_{in} + nV_{out}}{wL_s}\theta - i_{L0} \tag{3}$$

, which i_{L0} is the current of i_{Ls} *at* $\theta = 0$.



(a)



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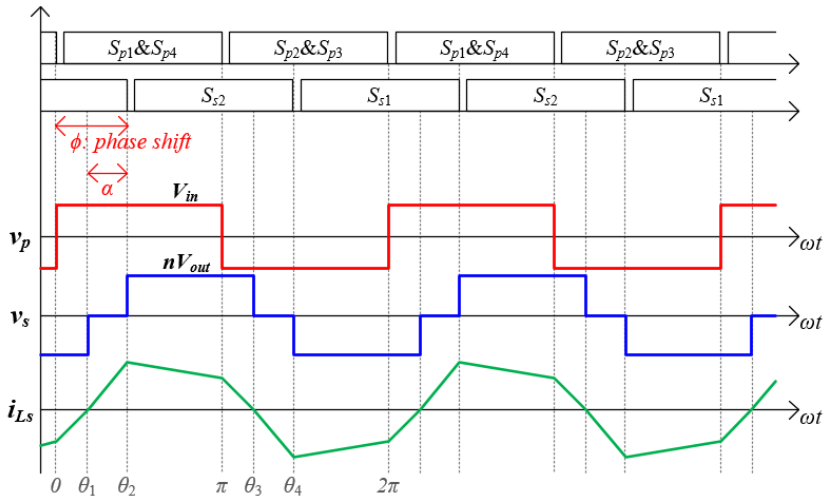


(c)

Fig. 2.6 Operational voltage, current waveforms of the semi-DAB converter when (a) m<1, (b) m=1, and (c) m>1

In interval 2 between $\theta_1(\phi-\alpha) < \theta < \theta_2(\phi)$, $v_p(\theta) = V_{in}$ and $v_s(\theta) = 0$. So, the current in interval 2 is shown as the equation (4),

$$i_{Ls}(\theta) = \frac{V_{in}}{wL_s}\theta - \frac{V_{in}}{wL_s}(\phi - \alpha) \tag{4}$$

In interval 3 between $\theta_2(\phi) < \theta < \pi$, $v_p(\theta) = V_{in}$ and $v_s(\theta) = nV_{out}$. So, the current in interval 3 is given in the equation (5),

$$i_{Ls}(\theta) = \frac{V_{in}-nV_{out}}{wL_s}(\theta - \phi) + i_{L1} \tag{5}$$

, which i_{L1} is current value of i_{Ls} at $\theta = \theta_2$. The i_{L0}, i_{L1}, and zero voltage interval α can be obtained using equations in each transition interval as below: (Details of the derivation follow in APPENDIX.A)

$$i_{L0} = \frac{V_{in}}{wL_s}(1+m)\frac{m\phi+(1-m)\pi}{m+2} \tag{6}$$

$$i_{L1} = \frac{V_{in}}{wL_s}\frac{2\phi-(1-m)\pi}{m+2} \tag{7}$$

$$\alpha = \frac{2\phi-(1-m)\pi}{m+2} \tag{8}$$

Current waveform in the interval 4 is the same as interval 1, only the direction of the current is reversed. So, in interval 4 between $\pi < \theta < \theta_3(\pi+\phi-\alpha)$, $v_p(\theta) = -V_{in}$ and $v_s(\theta) = nV_{out}$. The current in interval 4 can be obtained as the negative (3). On the same principle, interval 5 ($\theta_3 < \theta < \theta_4$) is the current in the opposite direction of interval 2, and interval 6 ($\theta_4 < \theta < \pi$) is similar to interval 3. Each interval operation processes are depicted in Fig. 2.7 during one cycle. Fig. 2.7(a) shows the current direction in interval 1 ($0 < \theta < \theta_1(\phi-\alpha)$), Fig. 2.7(b) describes the circuit and current flow in interval 2 ($\theta_1(\phi-\alpha) < \theta < \theta_2(\phi)$), Fig. 2.7(c) depicts the operational principles in interval 3 ($\theta_2(\phi) < \theta < \pi$), the working process of interval 4 ($\pi < \theta < \theta_3(\pi+\phi-\alpha)$) is shown as Fig. 2.7(d), Fig. 2.7(e) described the operational process of interval 5 ($\theta_3(\pi+\phi-\alpha) < \theta < \theta_4(\pi+\phi)$), and Fig. 2.7(f) shows the current path in interval 6 ($\theta_4(\pi+\phi) < \theta < \pi$).

The main difference in the operation principle of the Semi-DAB and DAB is that a zero voltage interval, during α, is generated in the secondary transformer voltage waveform, as shown in Fig. 2.7(b) and Fig. 2.7(e). This is because the current flow does not go to the upper leg but flows along the internal diode of the off switch as the switch is replaced by a diode. Therefore, a zero voltage interval is naturally created for the voltage of the transformer on the secondary side during α.

The power of semi-DAB can be derived by using current equations. Assuming as ideal semi-DAB converter, the input power is equal to the delivered output power. And the input power is derived as the

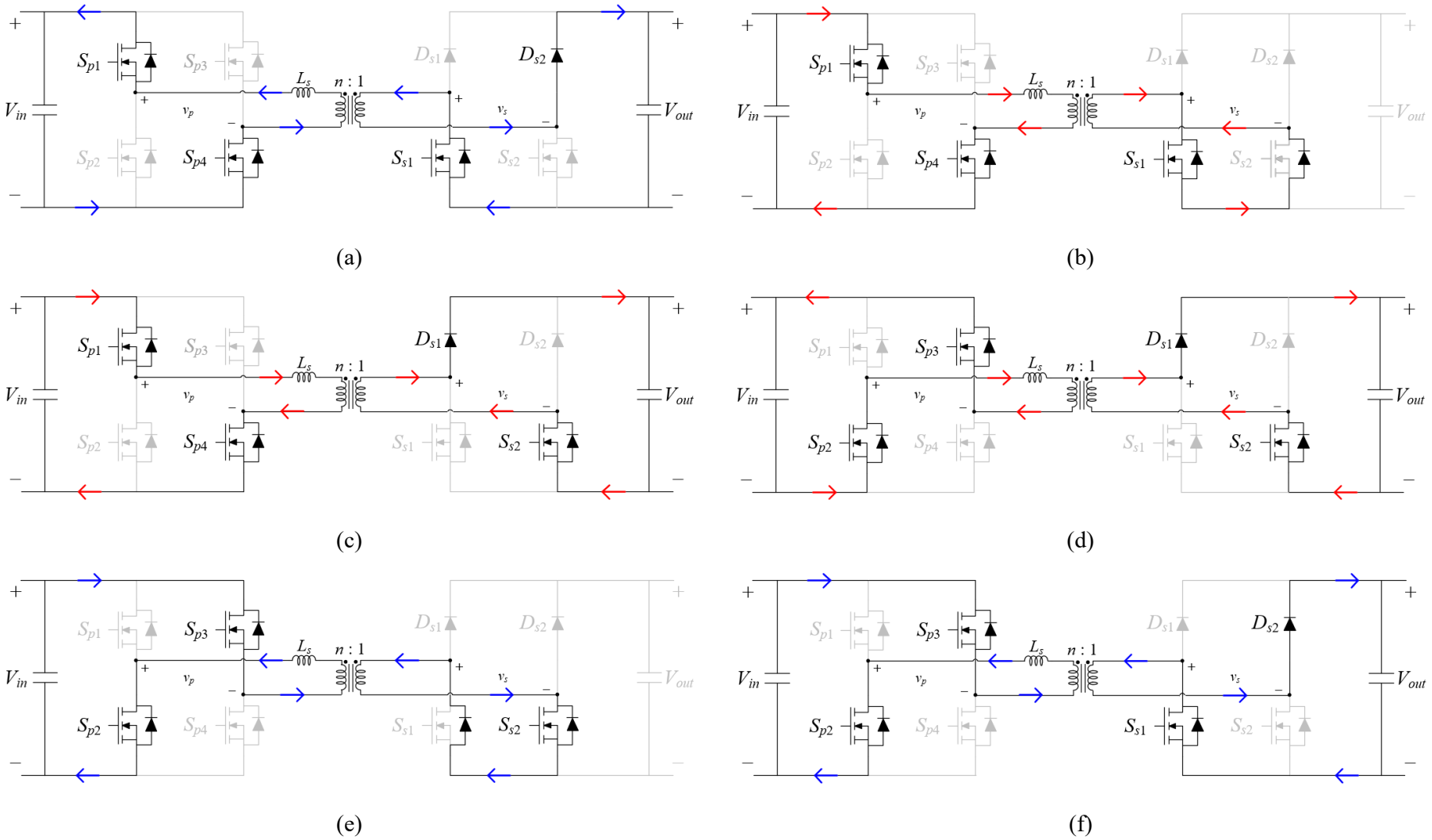


Fig. 2.7 Operational principles of semi-DAB in interval of (a) 0~θ_1, (b) θ_1~θ_2, (c) θ_2~π, (d) π~θ_3, (e) θ_3~θ_4, and (f) θ_4~2π.

product of the average input current and the average input voltage, as shown in equation (9)

$$P = i_{in,avg}V_{in} = i_{out,avg}V_{out} \tag{9}$$

, where the P is the output power [26]. The transferred power can be obtained as shown in (10) using the current equations already obtained and input voltage of the primary-side of the converter. (Details of the derivation follow in APPENDIX.B)

$$P = \frac{1}{2\pi}\frac{V_{in}^2}{(m+2)^2}\frac{1}{wL_s}[-2m(m^2+2m+2)\phi^2 + 4m(m^2+m+1)\pi\phi + m(1-m)(2m+1)\pi^2] \tag{10}$$

As derived in equation (10), the power in a semi-DAB can be expressed for voltage gain m and phase shift ϕ. Through this power equation, it is possible to design the appropriate leakage inductance by determining the transmittable power of the semi-DAB.

2.2 Power Loss Analysis of Semi-DAB

Before proposing a design to optimize the efficiency of the semi-DAB, it is necessary to analysis the loss of the semi-DAB in detailed. The loss of the converter can vary greatly depending on the load situation and the device or properties used. So, the loss of parasitic components that can be neglected are not considered, such as PCB conductor loss, dielectric loss, conducting wire losses or equivalent series resistance loss of capacitor. The loss of semi-DAB converter was analyzed by categorized into three losses, switching loss, conduction loss, and magnetic components loss [27]-[28].

First, switching loss is composed of the loss from the switches on the primary side and secondary side, and the reverse recovery loss of the diodes in secondary side. The switching loss is the loss of power that occurs while the switch is turn on or off, as the current and voltage intersect. The expressions related to switch loss in primary and secondary side are as below, equation (11)-(12),

$$P_{sw-P} = 2 \times \frac{1}{2}V_{Sp}I_{Sp}\left(t_{on} + t_{off}\right)f_{sw} \tag{11}$$

$$P_{sw-S} = \frac{1}{2}V_{Ss}I_{Ss}\left(t_{on} + t_{off}\right)f_{sw} \tag{12}$$

, which $P_{sw\text{-}P}$ is defined as switching loss of primary side, and $P_{sw\text{-}s}$ is defined as switching loss of secondary side. And V_{Sp} is voltage across of a primary side switch, I_{Sp} is current flowing through a primary side switch. V_{Ss} means the voltage across of a secondary side switch, and I_{Ss} is the current of a secondary side switch.

The t_{on} is the time intervals during ON operation of the switch, t_{off} is the time intervals during OFF operation of the switch. The t_{on} and t_{off} can be obtained from the datasheet of the switches. And f_{sw} is the switching frequency of this converter. In one period, only two switches on the primary side operate, so the switching loss on the primary side is doubled as shown in equation (11). On the secondary side, on the other hand, only one switch operates during one period, so it is expressed as (12). And the reverse recovery loss of the secondary side diodes is also included in the switching loss. The reverse recovery characteristic caused when the diode is converted from a forward bias to reverse bias condition. The diode reverse recovery loss on the secondary side is shown in expression (12) below,

$$P_{rev\_diode} = Q_f f_{sw} V_r = \left(Q_{rr} - \frac{I_{peak-rev}^2}{\frac{2di_f}{dt}} \right) f_{sw} V_r \tag{12}$$

, where P_{rev_diode} is reverse recovery loss of the secondary-side diodes of semi-DAB converter. Q_f means the recovered charge, f_{sw} is switching frequency, and V_r is reverse voltage of the diode. And Q_{rr} is the reverse recovery charge, $I_{peak-rev}$ is the reverse peak current. The reverse recovery charge, and differential of forward current are provided in datasheet of the diode.

The magnetic component loss consists of inductor and transformer loss. The inductor loss consists of DC copper loss, AC copper loss, hysteresis loss and Eddy current loss. DC copper loss and AC copper loss of inductor loss is due to windings, and hysteresis loss and Eddy current loss are due to core magnetic materials. But inductor has very los DCR, so DC copper loss are negligible. Therefore, the winding losses of the inductor can be approximated as shown in [29],

$$P_{wind} \cong I_{L\_rms}^2 \cdot R_{AC} \tag{13}$$

, where $I_{L,rms}$ is the rms current of the inductor, R_{AC} is AC resistance of the inductor winding component. Since there are many variables such as magnetic material, wire type, the number of litz wire, and diameter used for inductor fabrication, it is almost impossible to approximate by modeling, so it is obtained by directly measuring resistance in AC signal. The current flowing into the inductor is the same as the transformer, so the winding loss of the transformer is approximated as shown in expression(13). And the core loss can be obtained through Steinmetz's-formula [28]. When calculating core loss in semi-DAB, it is assumed that the current waveform is sinusoidal [30]-[31]. Because the derived Steinmetz's-equation is only valid for sinusoidal excitation as follows equation (14),

$$P_{core} = k f_{sw}^{\alpha} \hat{B}^{\beta} \tag{14}$$

TABLE I THE SYSTEM SPECIFICATIONS AND PARAMETERS USED FOR SEMI-DAB LOSS ANALYSIS

Parameter	Symbol	Value
Rated power	-	1.5 kW
Switching frequency	f_{sw}	50 kHz
Turn on time	t_{on}	54 ns
Turn off time	t_{off}	140.8 ns
Reverse recovery charge	Qrr	1000 μC
Inductor AC resistance	R_{AC}	100 mΩ
Peak magnetic flux density	$\hat{B}$	530 mT
Drain-source on-resistance	$r_{ds,on}$	65 mΩ
Forward voltage	V_f	1.61 V

, where $\hat{B}$ is the peak magnetic flux density, f_{sw} is switching frequency, and k, α, and β are material parameters. The material parameters k, α, and β can be obtained in a datasheet of core used.

The conduction loss is a loss caused by a current inevitably flow by the DCR of the component elements. In semi-DAB converter, the conduction loss occurs in the primary side switches and secondary side diodes and switches. The conduction loss of switch, almost as a MOSFET, is expressed by the following equation (15),

$$P_{mosfet-cond} = i^2 r_{ds,on} \tag{15}$$

, where the $P_{mosfet\text{-}cond}$ is the conduction loss of switch, i is rms current flowing the switch, and $r_{ds,on}$ is on-resistance of the MOSFET. In the semi-DAB converter, unlike the primary side, which consists of only switches, the secondary side has a combination of switches and diodes. The conduction loss of the diode is calculated as the product of the forward bias voltage and average current, and the related equation is as follows:

$$P_{diode-cond} = V_f \cdot I_{avg} \tag{16}$$

, where the $P_{diode\text{-}cond}$ means the conduction loss of diode, V_f is forward voltage of diode, and I_{avg} means the average current through the diode.

The system specifications and parameters used for the loss analysis of the semi-DAB analyzed using the previous equations are listed in TABLE I. The MOSFET referred to STW48N60DM2 datasheet from STMicroelectronics, and diode referred to DSEP29-06A datasheet from IXYS. And inductor and

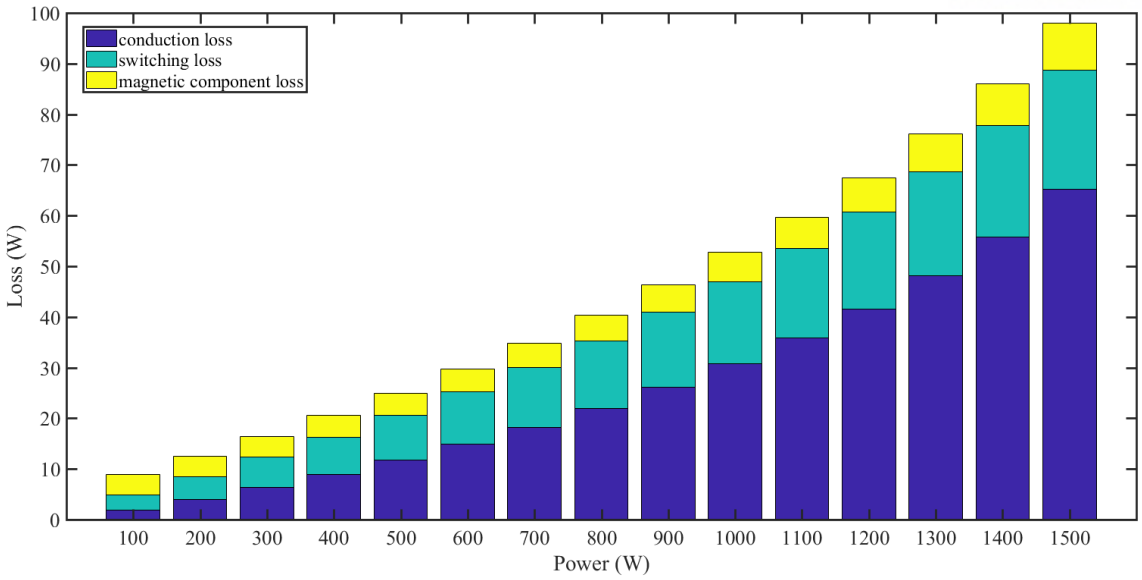


Fig. 2.8 Estimated loss varying output power of the semi-DAB converter

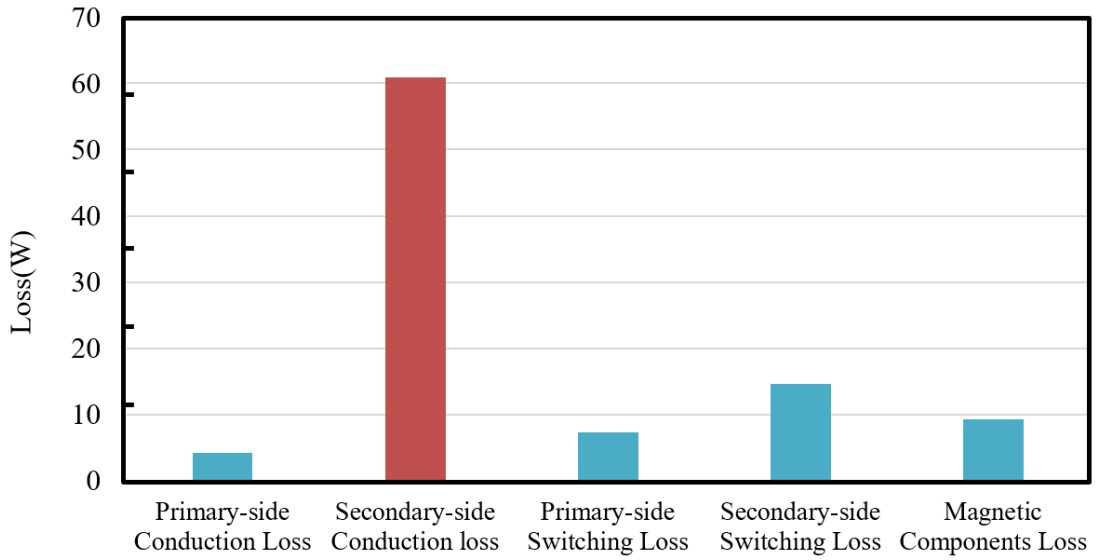


Fig. 2.9 Comparison of losses in full-load state (1500 W)

transformer core referred to EER6062S, ferrite core, datasheet from Samhwa Electronics. Fig. 2.8 shows the results of the analysis of the expected loss according to output power of the semi-DAB with the parameters of TABLE I. It can be seen that conduction loss is the most dominant from middle to high load what the charging application targeted. And Fig. 2.9 shows a comparison of losses for each type in a full-load (1500W) situation. This suggests that the conduction loss, especially the conduction loss on the secondary side, is the main cause of the semi-DAB losses in the situation.

The basic topology and working principle of the semi-DAB are presented in this chapter, and the numerical analysis for current and power are also derived. And, through the loss analysis of the semi-DAB converter, the dominant loss of the semi-DAB was covered in detail.

III. VOLTAGE GAIN DESIGN METHODOLOGY

In this chapter, the advanced voltage gain design methodology of transformers is proposed that can improve the efficiency of semi-DAB. The concept and principle of the proposed design methodology are explained, and the equations of the optimized voltage gain *m* is obtained through the proposed design method. The validity of the proposed design method is also verified by simulation, and feasibility can be demonstrated with a 1.5-kW prototype hardware experiment.

3.1 Impact of Voltage Gain Design

In most converter designs, the voltage gain is designed to 1 to minimize the peak current and rms current values to minimize conduction losses of the converter. In chapter 2, the current waveform when voltage gain is 1 or not 1 was examined in detail (Fig. 2.6). When the voltage gain is 1, the difference in voltage across the transformer is minimized, and the slope of the current becomes flat. That makes the peak current and rms current of the primary side smallest. Therefore, most converters are expected to have the highest efficiency if the transformer is designed with m=1. However, the converter of the charging application is characterized by giving a greater current to the output port, which makes the input voltage much greater than the output voltage to enable fast-charging. This means that there is also a difference between the current of primary and secondary side. Since the input power must be equal to the output power, in the charging applications, the current on the secondary side is two or three times greater than the primary side current.

The Fig. 3.1 presents a concept of proposed voltage gain design to increase the efficiency of the semi-

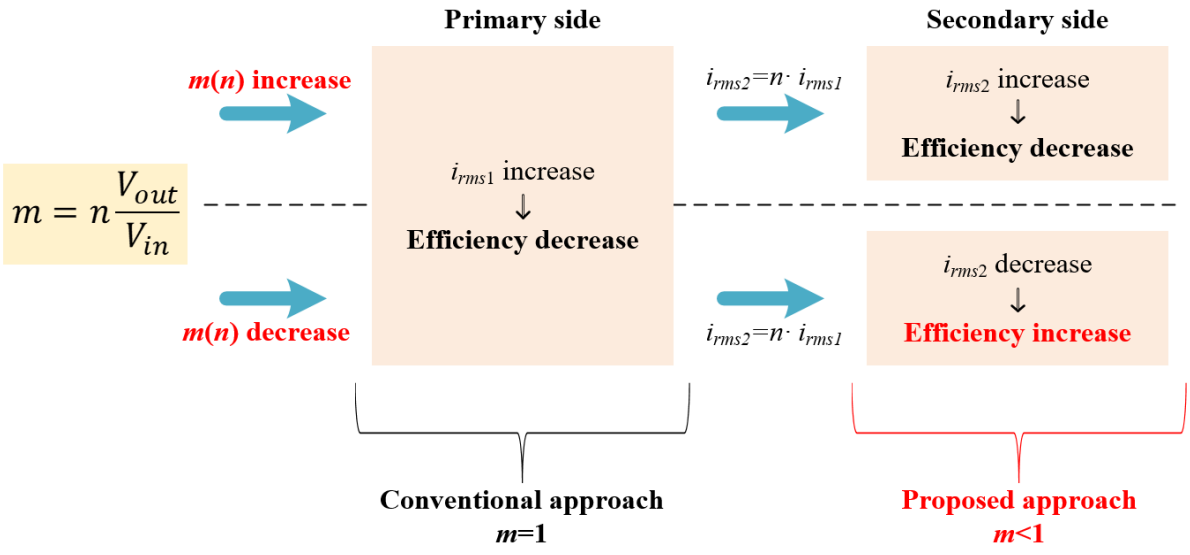


Fig. 3.1 Conceptual diagram of proposed voltage gain design to optimize efficiency of the semi-DAB

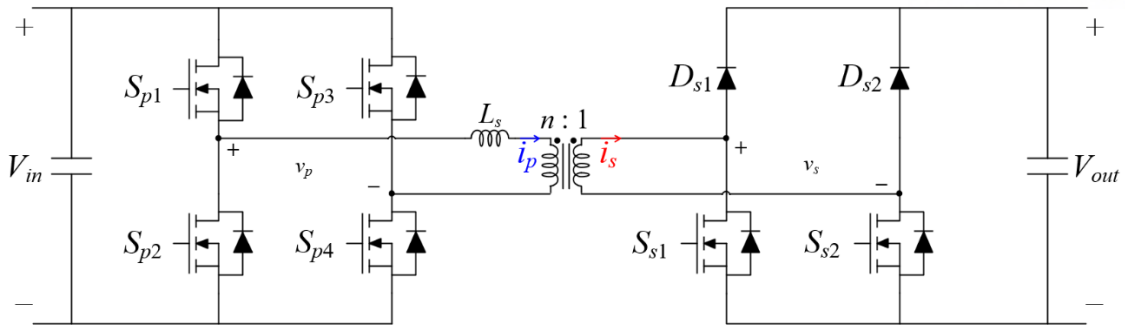


Fig. 3.2 The connection between the primary and secondary side current of the semi-DAB

DAB converter. As described above, in the conventional transformer voltage gain design, when *m* is smaller than 1 or larger were considered not good in efficiency because the rms current of the primary side becomes larger. However, since the rms current on the secondary side is multiplied by the transformer turn ratio (*n*) by the rms current on the primary side, if m is less than 1, the rms current on the secondary side can be smaller than the original value. Fig. 3.2 shows the relationship between the primary and secondary current of semi-DAB in a circuit. Because it is connected by a transformer, multiplying the current on the primary side by n, which is the turn ratio of the transformer, will result in the current of the semi-DAB converter on the secondary side. The derived relation between the rms current on primary side and secondary side is as follows,

$$i_{s,rms} = \sqrt{\frac{1}{T}\int_0^T i_s^2 dt} = \sqrt{\frac{1}{T}\int_0^T \left(n \cdot i_p\right)^2 dt} = n\sqrt{\frac{1}{T}\int_0^T i_p^2 dt} = n \cdot i_{p,rms} \tag{17}$$

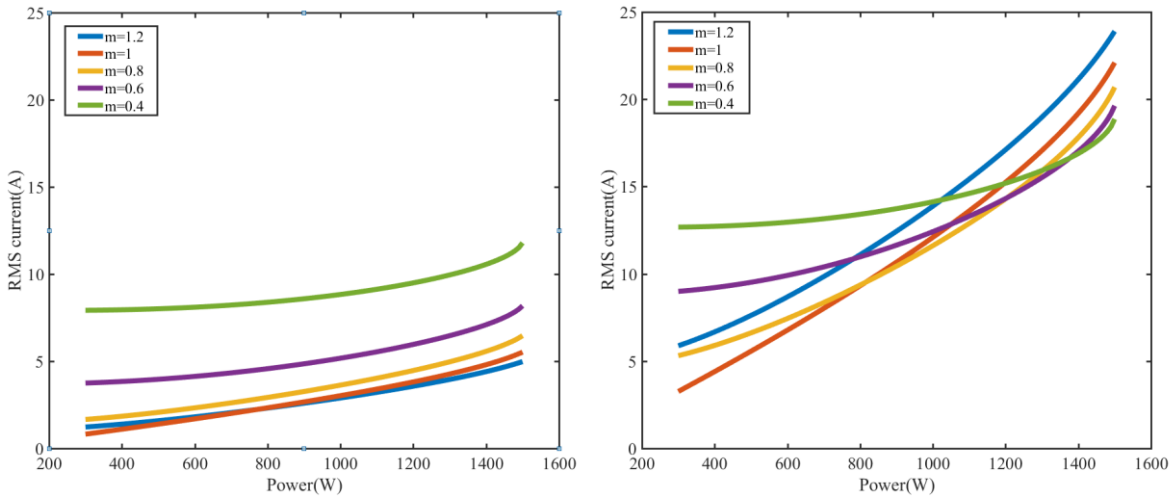
, where $i_{p,rms}$ is primary rms current of the semi-DAB, and $i_{s,rms}$ means secondary side rms current of the semi-DAB. Since it was confirmed that the conduction loss of the secondary side is the most dominant loss in the semi-DAB, the reduction of the rms current of the secondary side according to the proposed voltage gain design method reduces the conduction loss of the secondary side, leading to an increase in efficiency of the semi-DAB. The rms current on the primary is slightly increase, but since the current value on the secondary side is much larger, the rms current reduced on the secondary side is larger, reducing the conduction loss in the overall switch.

The conduction loss of the diode on the secondary side is confirmed previously that there is a relationship between the average current. The average current on the secondary side is also expressed as the product of the turn ratio of the transformer and the average current value on the primary side, as shown in equation (18),

$$i_{s,avg} = \frac{1}{T}\int_0^T i_s dt = \frac{1}{T}\int_0^T n \cdot i_p dt = n \cdot \frac{1}{T}\int_0^T i_p dt = n \cdot i_{p,avg} \tag{18}$$

TABLE II PARAMETERS AND 1SYSTEM SPECIFICATIONS FOR ANALYSIS OF THE PROPOSED VOLTAGE GAIN METHODOLOGY

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Output voltage	V_{out}	95 V
Turn ratio	n:1	1.6 ~ 4.8
Voltage gain	m	0.4 ~ 1.2
Rated power	-	max 1500 W
Switching frequency	f_{sw}	50 kHz



(a) (b)

Fig. 3.3 The simulated (a) primary side rms current, and (b) secondary side rms current for each load according to voltage gain

, where the $i_{s,avg}$ is the average current of the secondary side, and $i_{p,avg}$ is the average current of the primary side of the semi-DAB.

Using the equations (3)-(8), (17) and (18), the simulated rms current value for each load according to voltage gain was analyzed with MATLAB, an engineering software that provides a numerical and programming environment developed by MathWorks Inc., and it is shown in Fig. 3.3. The information on the system specification used to analyze and simulate the rms current on each side is shown in TABLE II. Fig. 3.3 (a) shows the primary side rms current at each load condition according to various voltage gain (m = 0.4 ~ 1.2), and Fig. 3.3(b) presents the secondary side rms current at each load condition according to various voltage gain (m = 0.4 ~ 1.2). The rms current on the primary side can be seen to increase as the voltage gain decreases, but on the secondary side rms current decreases as the voltage gain decreases. As a result, the conduction loss of the semi-DAB requires a combination of the

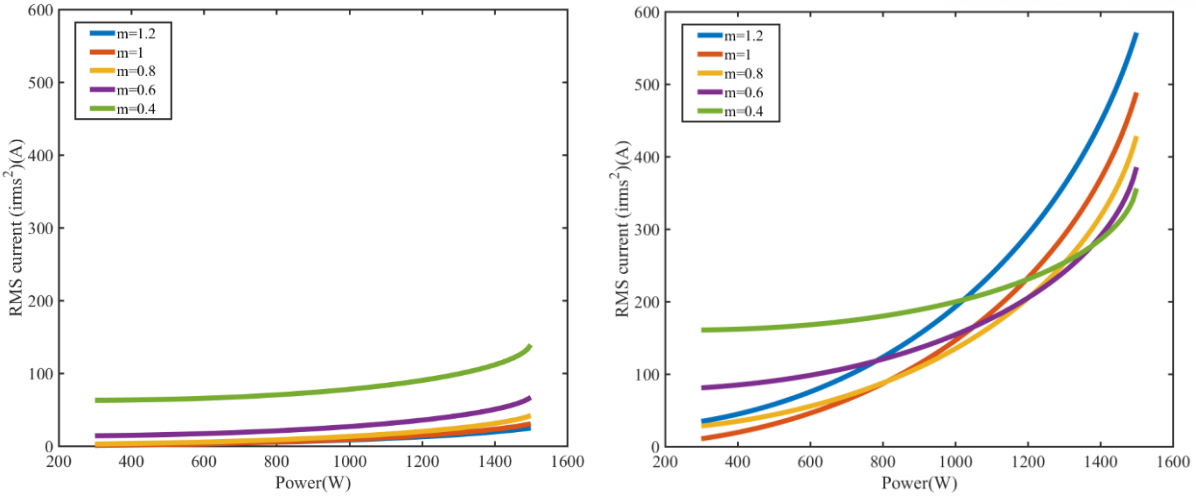


Fig. 3.4 The calculated squared (a) primary side rms current, and (b) secondary side rms current for each load according to voltage gain

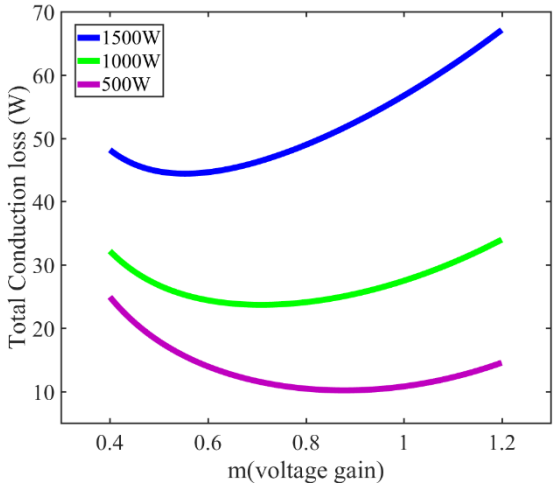


Fig. 3.5 Changes in the conduction loss of the specific load condition varying voltage gain

rms current on the primary side and the rms current on the secondary side to find the most appropriate optimized voltage gain value.

Since the conduction loss in the semi-DAB is related to equation (15), it is more appropriate to consider the square of rms current on primary and secondary side. Fig. 3.4 shows that the simulated squared primary side rms current, and squared secondary side rms current for each load varying voltage gain. The lower the voltage gain, the smaller rms current on the secondary side. However, if the voltage gain is too low, the rise of the rms current on the primary side becomes large, so the total conduction loss may increase. Fig. 3.5 shows the result of predicting total conduction loss with the rms current value of each side simulated and the parameters of TABLE II, with varying load-condition and voltage gain. In full-load condition (1500W), the total conduction loss is minimum when the voltage gain is

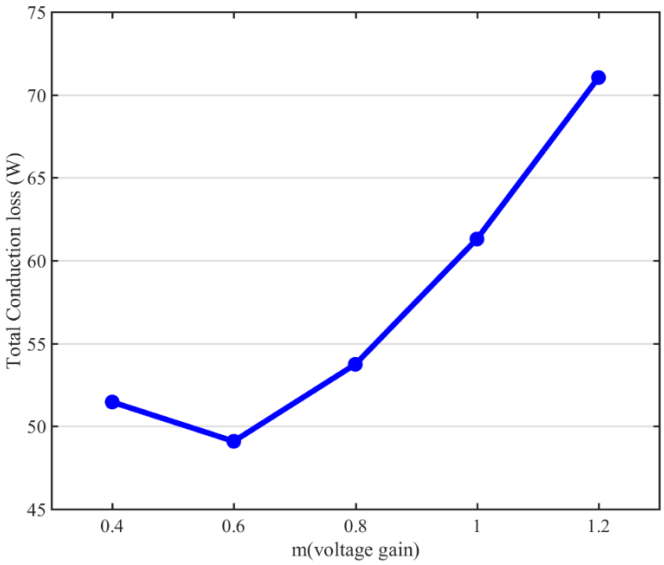


Fig. 3.6 The predicted total conduction loss with varying voltage gain in full-load condition

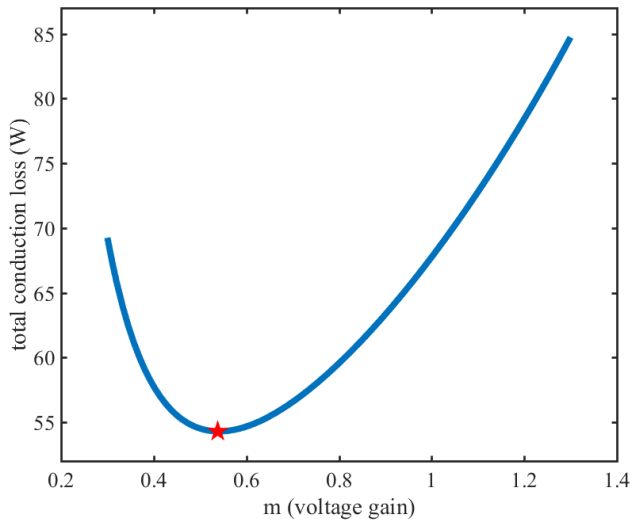


Fig. 3.7 The total conduction loss curve varying the voltage gain to find optimal *m*

about 0.6, when the middle-load condition (1000W), the minimum conduction loss can be obtained when the voltage gain is about 0.7. In light-load condition (500W), it can be expected that the minimum conduction loss can be obtained when the voltage gain is 0.9~1. The optimal voltage gain value to obtain a minimum conduction loss in accordance with the load condition varies, considering the situations of charging application, it is advantageous to design close to the optimum voltage gain at high load. This is because, in a charging application, when a large current flow in the output port, conduction loss is largest, so it can be referred to as worst-case when high-load condition.

In EV charging load condition, most of the high-speed charging is performed at a heavy load condition, and the general charging is performed at a middle-to-high load. Charging at low load is not dominant condition and loss at light load condition is small because the power at light load is small.

Charging performance in the light load state is less important than high load condition because the low load on the EV battery charge converter means a state of charge of more than 80 % of the battery capacity. However, it would like to optimize the load condition, there must be information about the load condition that works when charging the battery. If there is a data set on which load is most charged, the load condition can be optimized by giving a large weight factor in the order. In this optimized load, the most optimized voltage gain can be obtained, and the transformer and hardware can be configured using this optimized voltage gain.

Fig. 3.6 shows that the predicted total conduction loss with varying voltage gain in full-load condition, which is worst case of the 1.5 kW semi-DAB converter. When full-load condition, m=0.6 is most optimized voltage gain value that can minimize the conduction losses of the semi-DAB converter.

3.2 Proposed Voltage Gain Design Method to Minimize Conduction Loss

The design methodology of the voltage gain value that can minimize the conduction losses of the proposed semi-DAB was examined. It describes a method for more accurately derive an optimized voltage gain design method to mathematically proposed to minimize the conduction loss of semi-DAB converter. First, when expressing the total conduction loss in the semi-DAB as an equation as follows,

$$P_{tot-cond-loss} = \left(i_{p,rms}^2 \cdot r_{ds,on1}\right) + \left(i_{s,rms}^2 \cdot r_{ds,on2}\right) + \left(V_f \cdot I_{s,avg}\right) \tag{19}$$

, where the $P_{tot\text{-}cond\text{-}loss}$ is total conduction loss of the semi-DAB designed, $i_{p,rms}$ is the rms current of the primary side, and $i_{s,rms}$ means the rms current of the secondary side. And the $r_{ds,on}$ is the drain-source on-resistance of the switch in semi-DAB converter, V_f is forward voltage drop of the diodes on secondary side, and $I_{s,avg}$ means the average current of the secondary side. An equation (20) can be obtained, if the equation (17) and (19) can be refined.

$$P_{tot-cond-loss} = \left(2r_{ds,on1} + n^2 r_{ds,on2}\right)\frac{1}{\pi}\left[\int_0^{\phi-\alpha} i_1^2 d\theta + \int_{\phi-\alpha}^{\phi} i_2^2\, d\theta + \int_{\phi}^{\pi} i_3^2\, d\theta\right] + V_f \times I_{s,avg} \tag{20}$$

, which i1 means the equation (3), i2 is equal to the equation (4), and i3 means the equation (5). And the average current on the secondary side of the semi-DAB can be calculated as shown in (21), as below,

$$I_{s,avg} = \frac{n}{\pi}\left[-i_{L0}\phi + (i_{L0} + i_{L1})(\pi - \phi + \alpha)\right] \tag{21}$$

, where the i_{L0}, i_{L1}, and α are presented in equation (6)-(8), and ϕ means phase shift angle of the semi-DAB converter. To find the optimal voltage gain point m_{opt}, by combining the above equations, it is

TABLE III PARAMETERS AND SYSTEM SPECIFICATIONS FOR SIMULATION OF THE PROPOSED VOLTAGE GAIN METHODOLOGY

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Output voltage	V_{out}	95 V
Turn ratio	n:1	1.6, 2.4, 3.2, 4, 4.8
Voltage gain	m	0.4, 0.6, 0.8, 1, 1.2
Rated power	-	500 W, 1000 W, 1500 W
Power inductor	$L_{m=0.4}$	85.23 μH
	$L_{m=0.6}$	120.96 μH
	$L_{m=0.8}$	151.03 μH
	$L_{m=1}$	175.49 μH
	$L_{m=1.2}$	194.6 μH
Switching frequency	f_{sw}	50 kHz

necessary to find m with the derivative of equation (20) equal to zero. So, derived mathematical equation of optimal m_{opt} is expressed in a 4th order numerator and 2nd order denominator. It can be assumed to be a form of 2nd order equation, therefore, the optimal m_{opt} point can be calculated with on point in numerical analysis. Fig. 3.7 presents the optimal voltage gain m according to the total conduction loss as a function, and display the optimal m value which has the lowest conduction loss to the marker. The lowest point was obtained using MATLAB's mathematical analysis function (diff and solve). The optimal value of voltage gain m_{opt}, which minimizes the conduction loss of semi-DAB, was found to be 0.5382. However, for practical design, when designing and verifying actual hardware, the voltage gain was divided into 0.2 units and designed as 0.6 as the optimal voltage gain point.

In addition, in the design of transformer turn ration, all load conditions must be covered with a single transformer, which cannot be changed for various each load conditions. Therefore, the voltage gain was obtained by considering the load condition at the highest load with the highest loss, and having the minimum loss at the high load. Also, even if the optimized voltage gain value is a decimal point, there is such a limitation because the voltage gain cannot be adjusted to the correct value when making the transformer. Therefore, considering these limitations, the voltage gain of the transformer was designed with a separation by 0.2.

3.3 Simulation Results

To verify the effectiveness of the proposed voltage gain design methodology, a 1.5 kW semi-DAB was implemented through PSIM simulator. PSIM is the accurate power electronics design and circuit

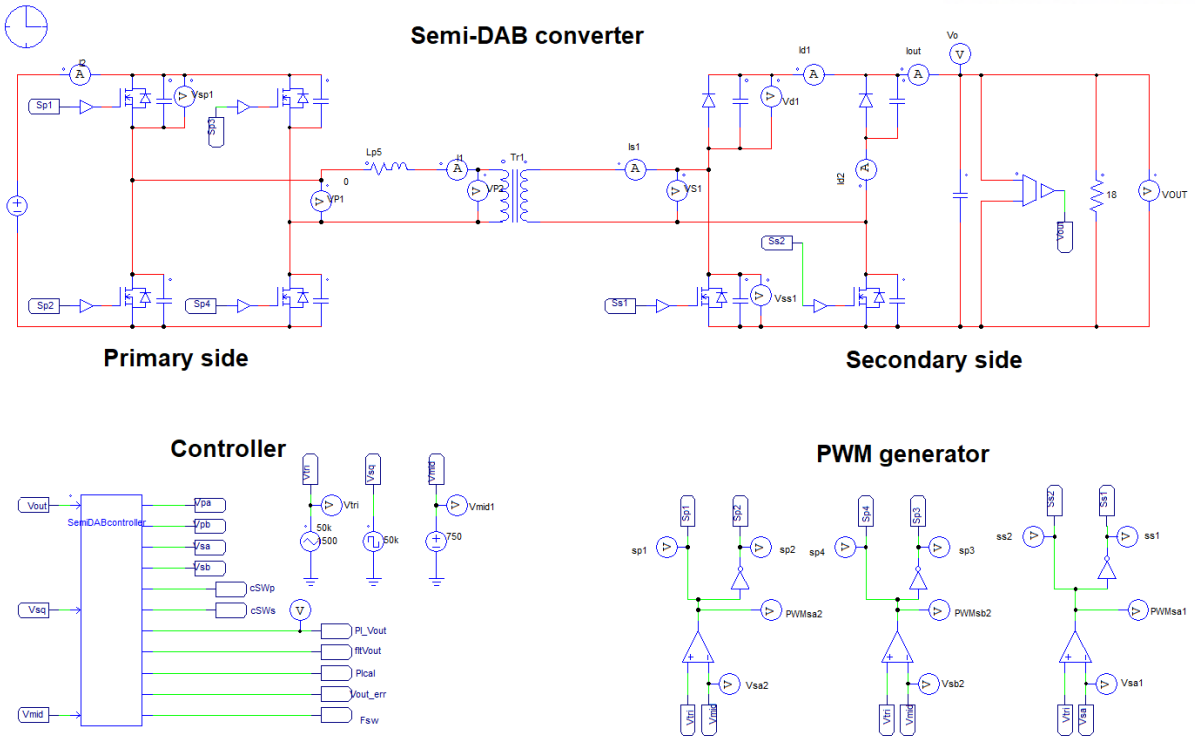
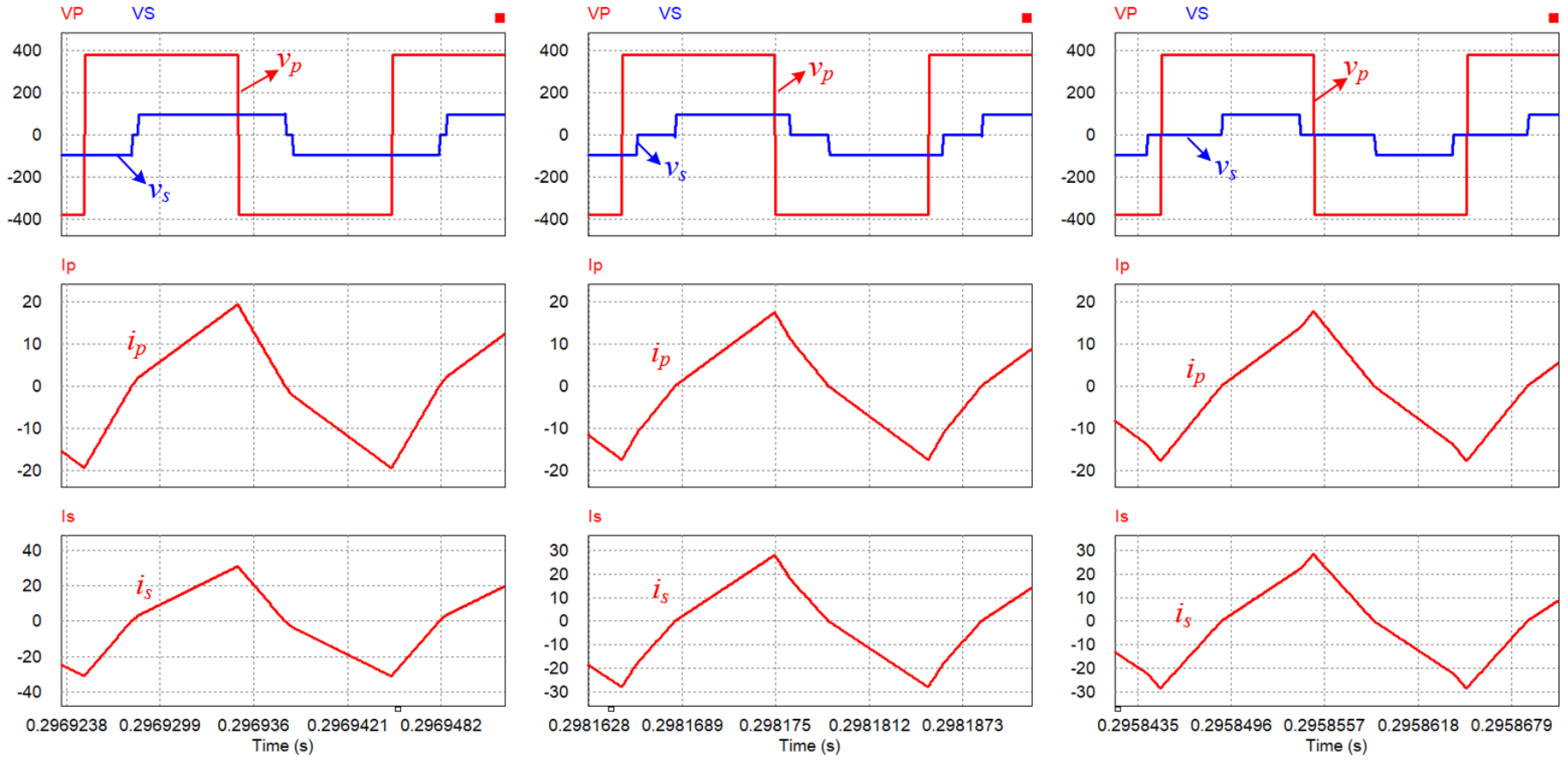


Fig. 3.8 The semi-DAB converter implemented in PSIM

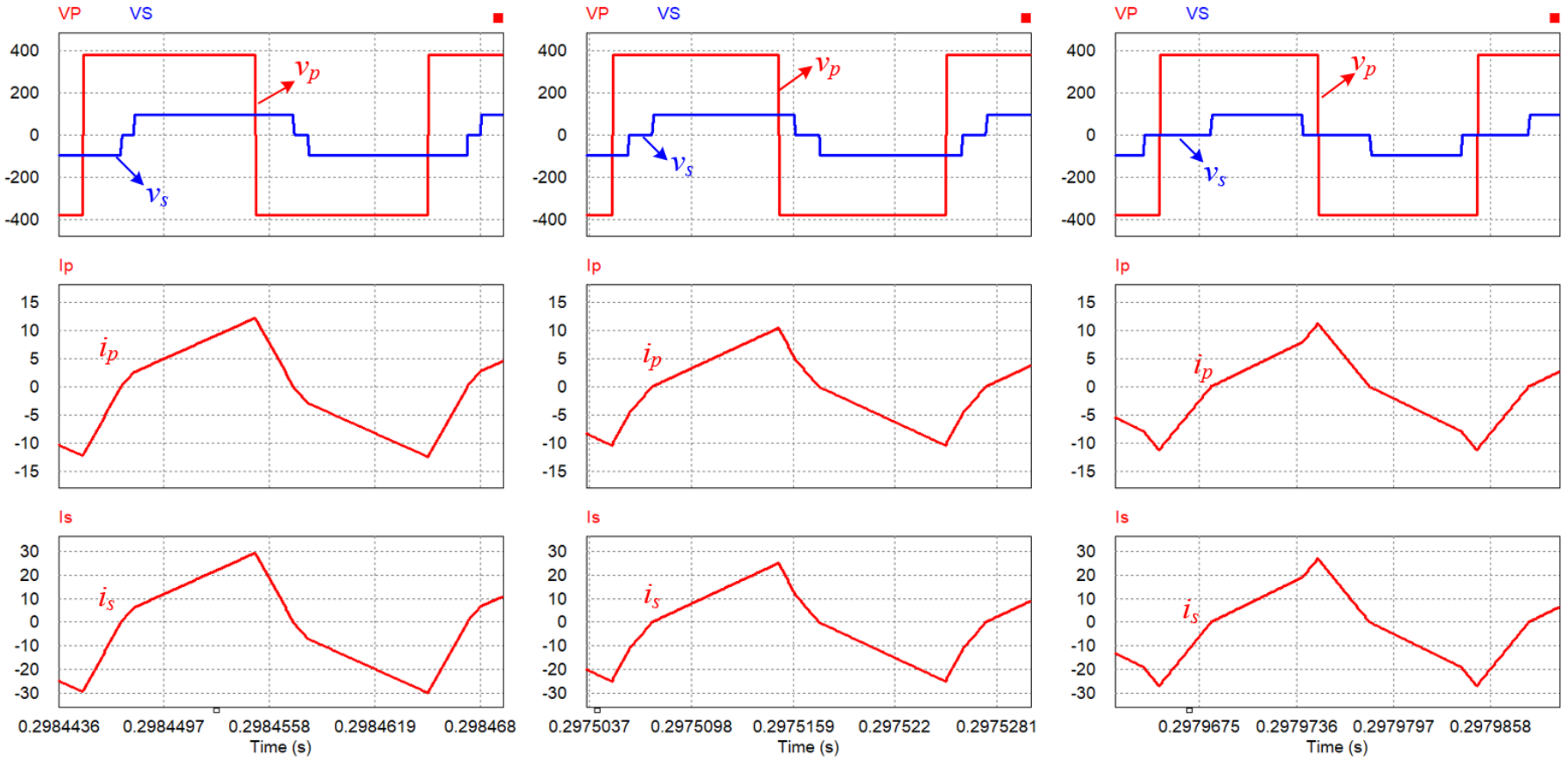
and system level simulator. from Powersim Inc. Based on the parameters and system specifications listed in TABLE III, a 1.5 kW semi-DAB circuit was implemented. Input voltage is 380 V, which is the default voltage of the DC distribution, and output voltage set to 95 V, which is 4 times lower than the input voltage. Because, for high-speed charging in the charging application, the voltage at the input stage is set over 3 times higher than the voltage at the output stage. Since the rms current changes of the primary and secondary side according to the voltage gain have be observed, a transformer having various voltage gains is used. In addition, since the value of the power inductor for matching the power rate of 1500 W according to the voltage gain of each transformer is changed, five power inductors are required ($L_{m=0.4} \sim L_{m=1.2}$). And the switching frequency of the designed semi-DAB converter was set to 50 kHz. The circuit implemented using PSIM is shown in Fig. 3.8. There are existed in semi-DAB converter power stage including primary side and secondary side, controller, and PWM generator. As shown in Fig. 3.8, the H-bridge was constructed using four MOSFET devices on the primary side, and the semi-bridge was constructed using two diode devices on the upper leg and two MOSFET devices on the lower leg of the secondary side for semi-DAB converter.

From Fig. 3.9 to Fig. 3.13 illustrates the simulation results of the voltage and current waveforms of primary side and secondary side with varying voltage gain m. The v_p in the figure means the primary port voltage, v_s in the figure is the secondary port voltage. And the i_p presents the primary side current waveform, and i_s means the secondary side current waveform of the semi-DAB. Fig. 3.9 shows the voltage across the transformer for each load, 1500 W, 1000 W, and 500 W, when m=0.4 and the current



(a) (b) (c)

Fig.3.9 The simulation results of voltage, current waveforms of primary side and secondary side when m=0.4, (a) 1500 W, (b) 1000 W, (c) 500 W



(a) (b) (c)

Fig. The simulation results of voltage, current waveforms of primary side and secondary side when m=0.6, (a) 1500 W, (b) 1000 W, (c) 500 W

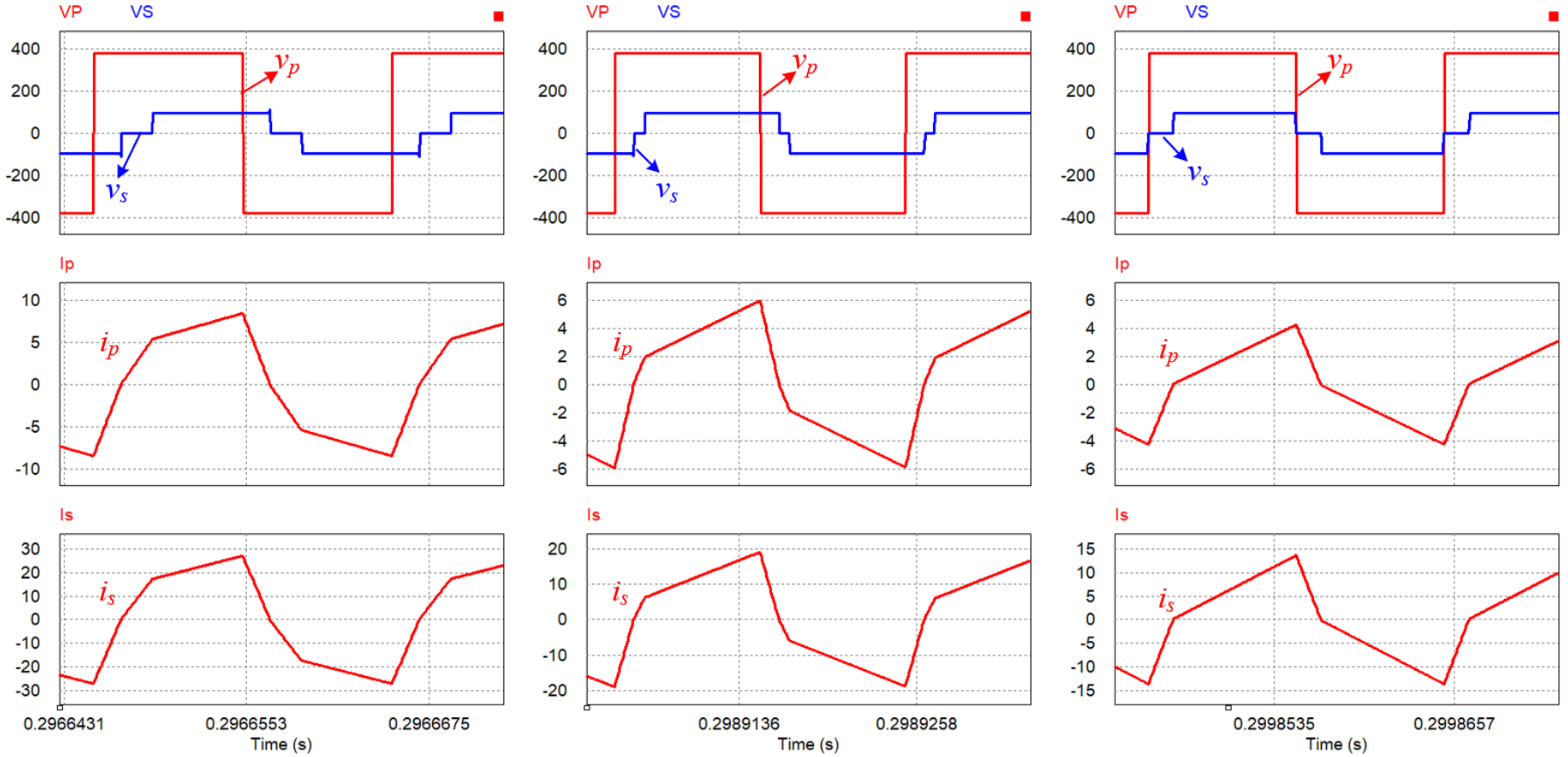
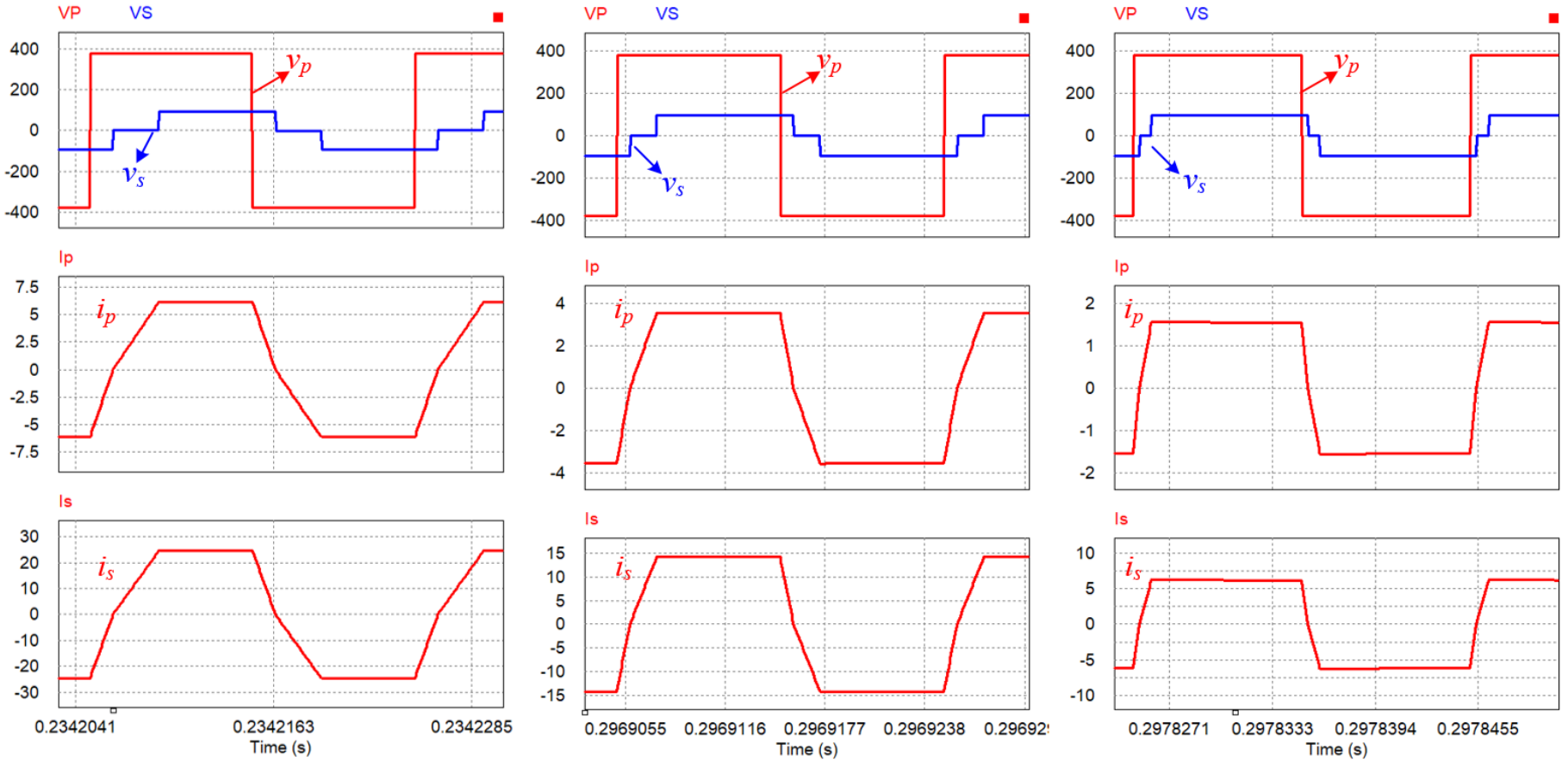
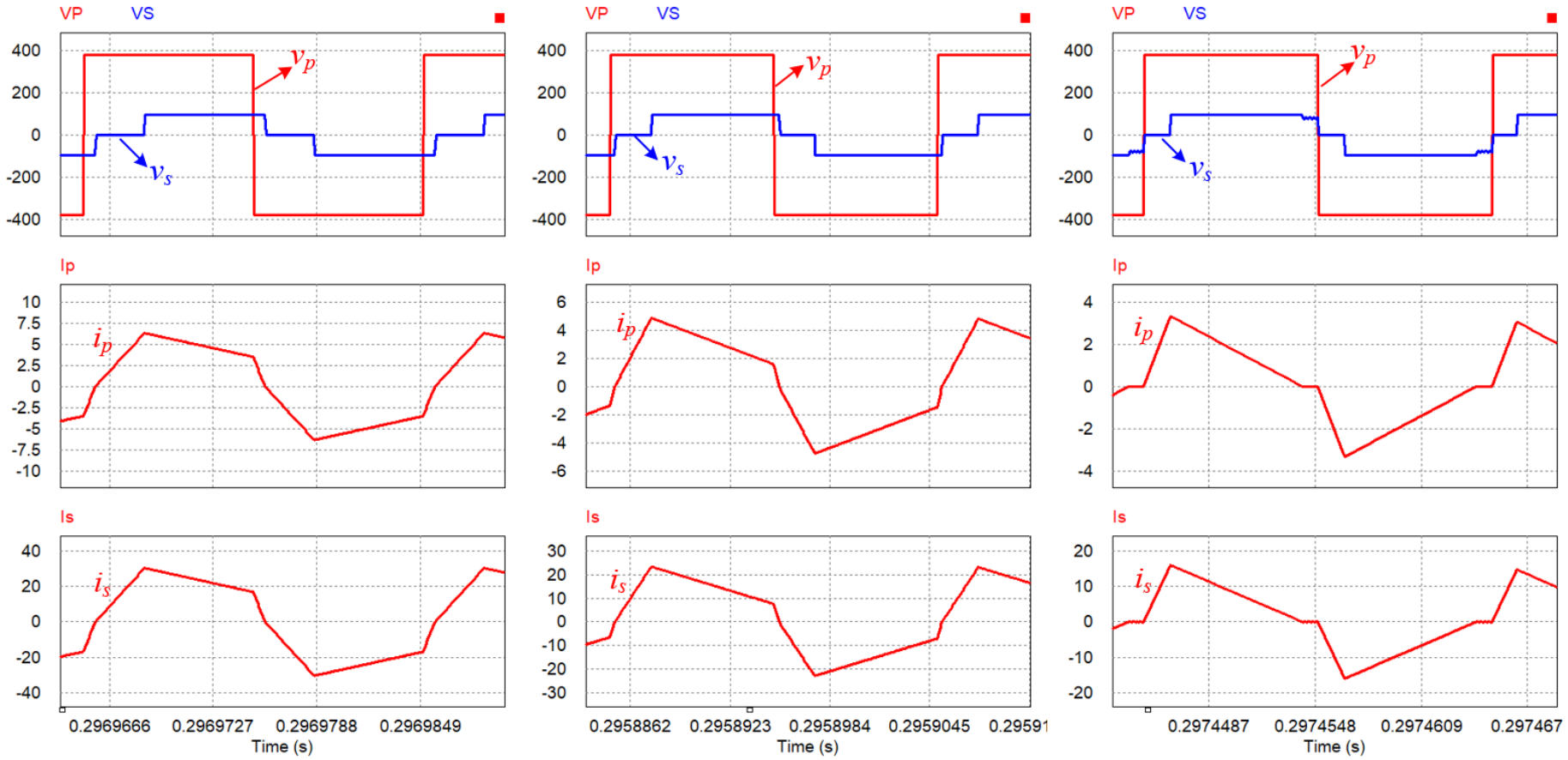


Fig. 3.11 The simulation results of voltage, current waveforms of primary side and secondary side when m=0.8, (a) 1500 W, (b) 1000 W, (c) 500 W



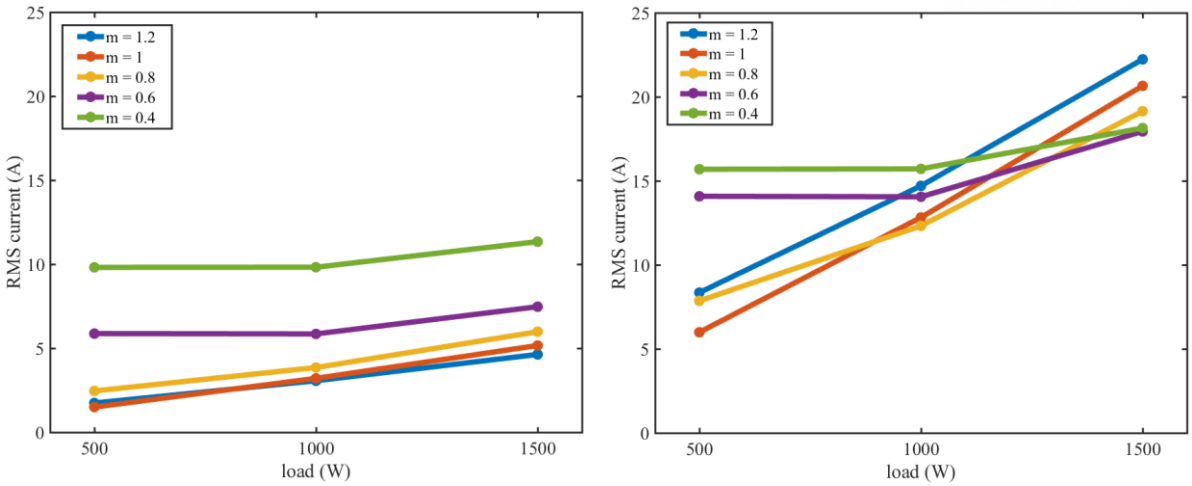
(a) (b) (c)

Fig. 3.12 The simulation results of voltage, current waveforms of primary side and secondary side when *m*=1, (a) 1500 W, (b) 1000 W, (c) 500 W



(a) (b) (c)

Fig. 3.13 The simulation results of voltage, current waveforms of primary side and secondary side when m=1.2, (a) 1500 W, (b) 1000 W, (c) 500 W



(a) (b)

Fig. 3.14 The simulated results with PSIM (a) primary side rms current, and (b) secondary side rms current for each load according to voltage gain

waveform on the primary and secondary sides. Fig. 3.9 (a) depicts the voltage and current waveforms at full-load, 1500 W, Fig. 3.9 (b) is 1000 W, and Fig. 3.9 (c) show the waveforms when load is 500 W. And Fig. 3.10 illustrates the current and voltage waveforms for each load condition when voltage gain is equal to 0.6. The Fig. 3.10 (a) is the case of 1500 W load condition, Fig. 3.10 (b) is in the case of 1000 W and Fig. 3.10(c) shows the 500 W load condition. Fig. 3.11 (a), (b), and (c) shows the voltage and current waveforms when the voltage gain m=0.8. Fig. 3.11 (a) is 1500 W load condition, (b) is 1000 W load condition, and (c) shows under the 500 W load condition. Fig. 3.12 (a) presents the voltage across the transformer of the semi-DAB, the primary side current and secondary side current waveforms under 1500 W load condition when the m=1. Fig. 3.12 (b) shows the voltage and current waveforms when 1000 W load condition, and Fig. 3.12 (c) is when the 500 W load conditions with m=1. In m=1 condition, the current waveforms are most flat waveform. The Fig. 3.13 (a),(b), and (c) is 1500 W, 1000 W, and 500 W when the voltage gain m=1.2.

The results of extracting the rms values from the current waveforms of the primary and secondary sides obtained in Fig. 3.9 ~ Fig. 3.13 are shown in Fig. 3.14. It is well matched to the theoretical analysis of Fig. 3.3. Compared with the high load conditions, the smaller the voltage gain, the greater rms current on the primary side, but the smaller the rms current on the secondary side. However, since the current value on the secondary side has a greater effect on the total conduction loss of the semi-DAB than the current value on the primary side, it can be interpreted that the overall conduction losses can be reduced when the voltage gain getting smaller. However, since the current on the primary side will also increase significantly at any specific voltage gain point that minimizes conduction loss of the semi-DAB. In the next chapter will be verifying it as an experiment.

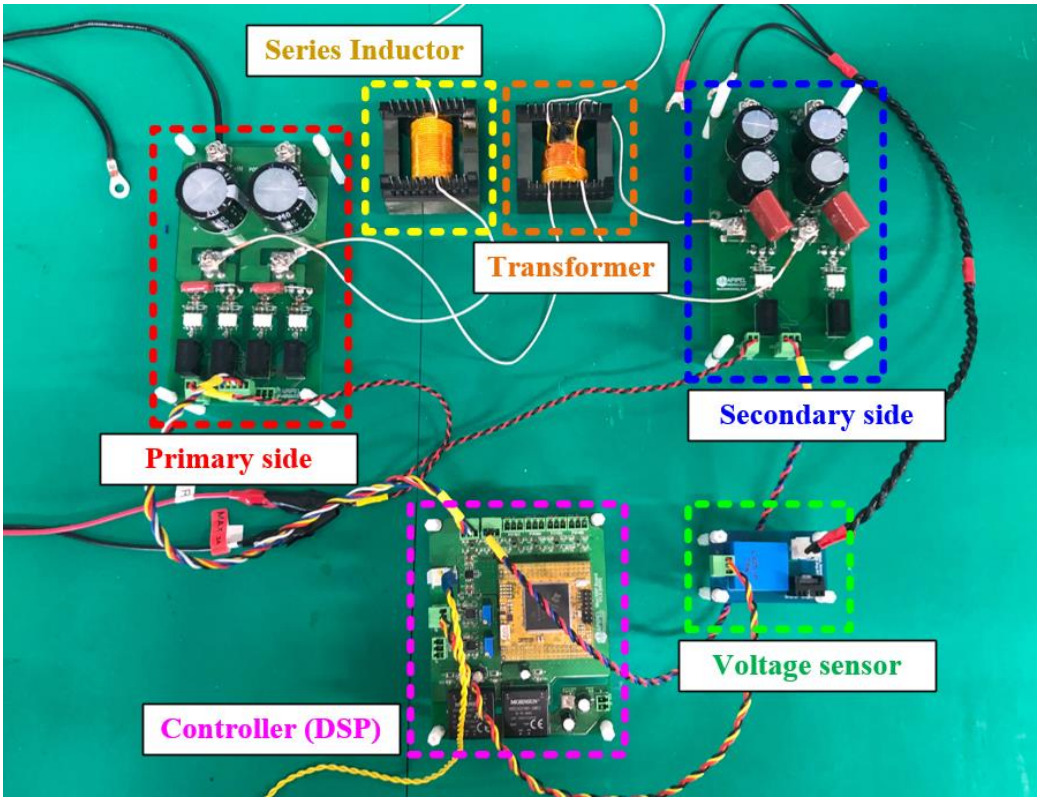


Fig. 3.15 1.5-kW semi-DAB converter prototype and experimental environment

3.4 Experimental Results

In order to verify that the proposed voltage gain design method can decrease the conduction loss and increase the efficiency of the semi-DAB converter, a implemented 1.5-kW prototype hardware was experimented. The implemented prototype of the semi-DAB is presented in Fig. 3.15. The hardware includes primary-side board and secondary-side board. In prototype hardware fast-recovery MOSFETs, STW48N60DM2 from STMicroelectronics, and high performance fast-recovery diodes, DSEP60-12A manufactured by IXYS, are used. And digital controller, TMS320F28335 from Texas Instruments, is used. Using the DSP, the switching modulation of the semi-DAB can be controlled. The ferrite cores are used in series inductor and transformer, which is EER6062S manufactured by Samhwa Electronics. And using the voltage sensor, sensing the output voltage to control the output voltage of semi-DAB.

The specification of the system used in hardware experiment are listed in TABLE IV. When designing the system before, it was designed to be similar to the ideal parameters of the designed TABLE III. However, since there are practical limitations in the production of hardware, it cannot be produced with the very same specification. For example, in the manufacture of transformers, the number of turns on the secondary side should be fixed, and the number of turns on the primary side should be changed to match the voltage gain, but the number of turns that match the design value cannot be set exactly. This

TABLE IV SYSTEM SPECIFICATIONS AND PARAMETERS FOR 1.5-kW PROTOTYPE HARDWARE OF THE SEMI-DAB CONVERTER

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Output voltage	V_{out}	95 V
Turn ratio	n:1	1.667, 2.5, 3.333, 4, 4.8333
Voltage gain	m	0.416, 0.625, 0.833, 1, 1.208
Rated power	-	500 W, 1000 W, 1500 W
Power inductor	$L_{m=0.4}$	82.78 μH
	$L_{m=0.6}$	110.8 μH
	$L_{m=0.8}$	139.62 μH
	$L_{m=1}$	165.79 μH
	$L_{m=1.2}$	183.69 μH
Switching frequency	f_{sw}	50 kHz

is because the turn number of the transformer must be wound with an integer number. The series inductor of the semi-DAB is also slightly different from the designed value for the same reason. However, since the power rate can be covered up to the maximum power only when the series inductance is slightly smaller than the designed value, the smallest inductance closest to the designed value can be used. Otherwise, by using larger inductance than the design value, it is not available to a maximum power rate.

1500 W, 1000W, and 500 W were tested using the manufactured semi-DAB converter, and the load was a passive load resistor. Because of the output voltage of 95 V, 1500 W is used for 6 Ω of resistor, 1000 W for 9 Ω, and 500 W for 18 Ω resistor. Each 1500 W, 1000 W, and 500 W was presented for full-load condition, middle load, and light load situations of designed semi-DAB converter having maximum power rate 1.5-kW. In full-load condition, the voltage and current capacity on input side is 380 V-4 A, and output side is 95 V-15.7 A. And the actual power rate in the charging application was several kW, but miniaturize to 1.5 kW for experiments that could be proceed in the laboratory-scale.

From Fig. 3.16 to Fig. 3.20, the figures present the experimental waveforms with varying voltage gain and load conditions. In these figures, v_p means the primary side voltage of transformer, v_s is the secondary side voltage of transformer. And i_p presents the primary side current waveform, and i_s the secondary side current. Compared with the simulation waveforms from Fig. 3.9 to Fig. 3.13, the voltage and current waveforms appears similarly with the experiment results. The Fig. 3.16 shows the voltage and current waveforms when the voltage gain is 0.4, Fig. 3.17 presents the waveforms when the m = 0.6, Fig. 3.18 is when the voltage gain is 0.8, Fig. 3.19 depicts the voltage and current when m=1, and Fig. 3.20 shows the waveforms when the voltage gain is 1.2.

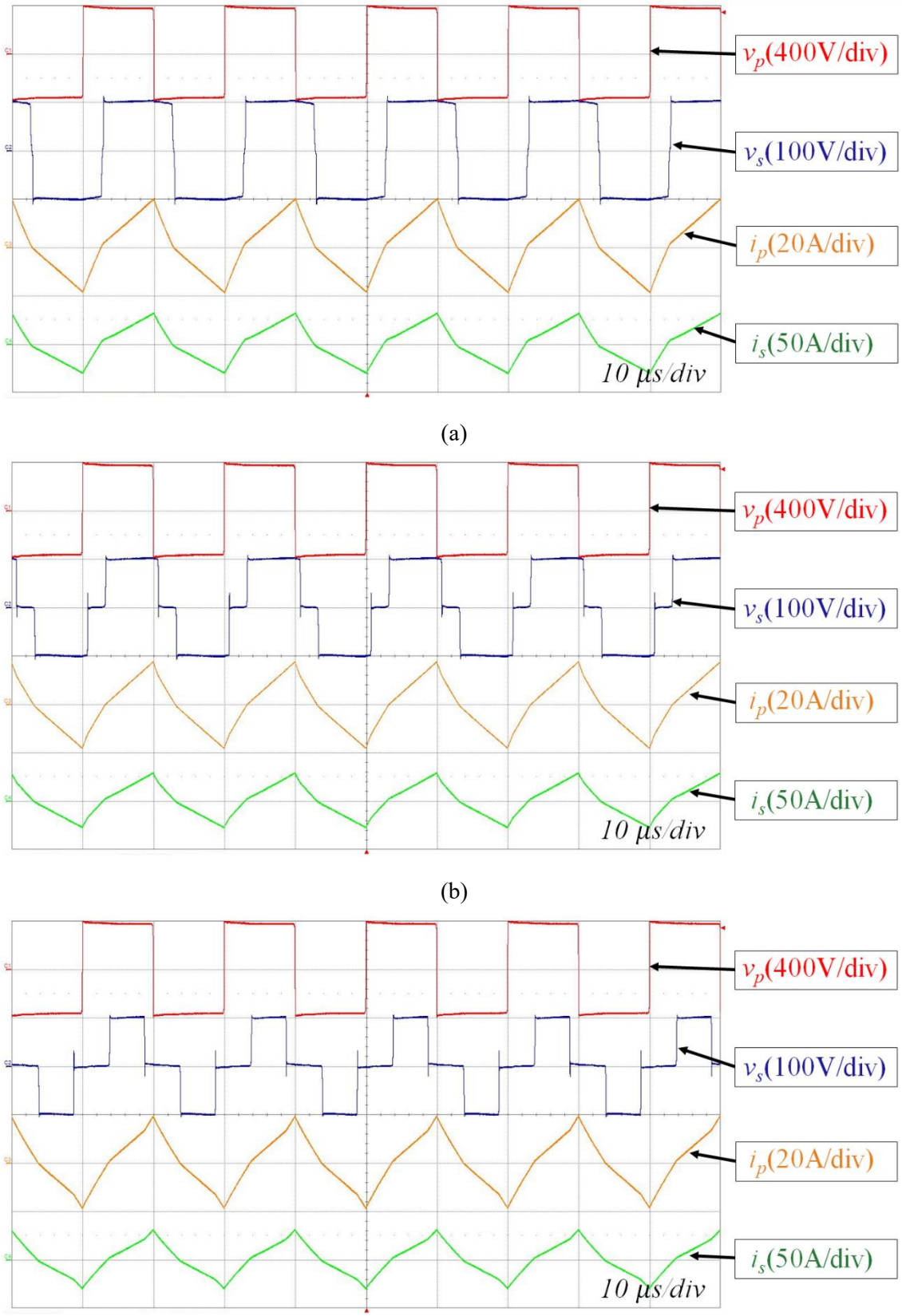
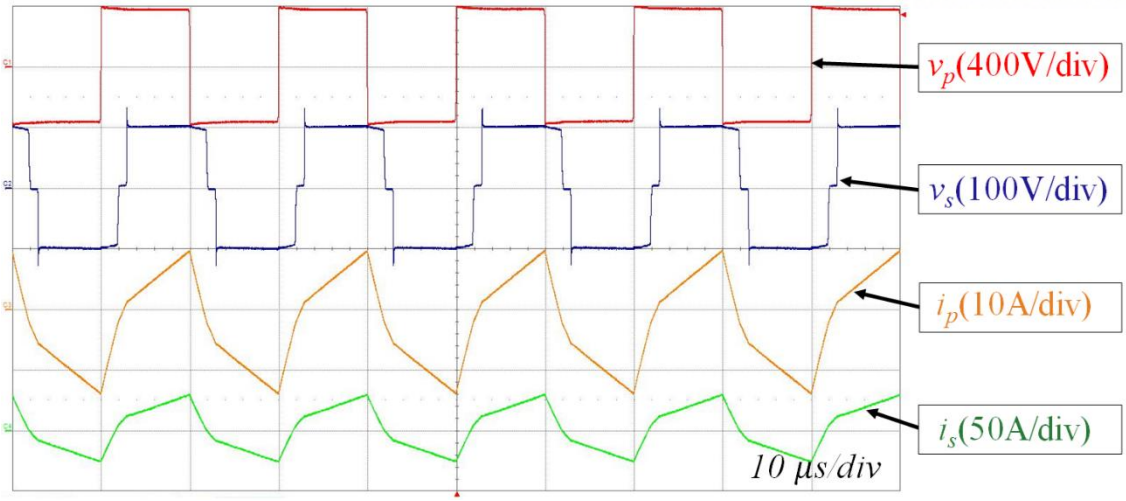
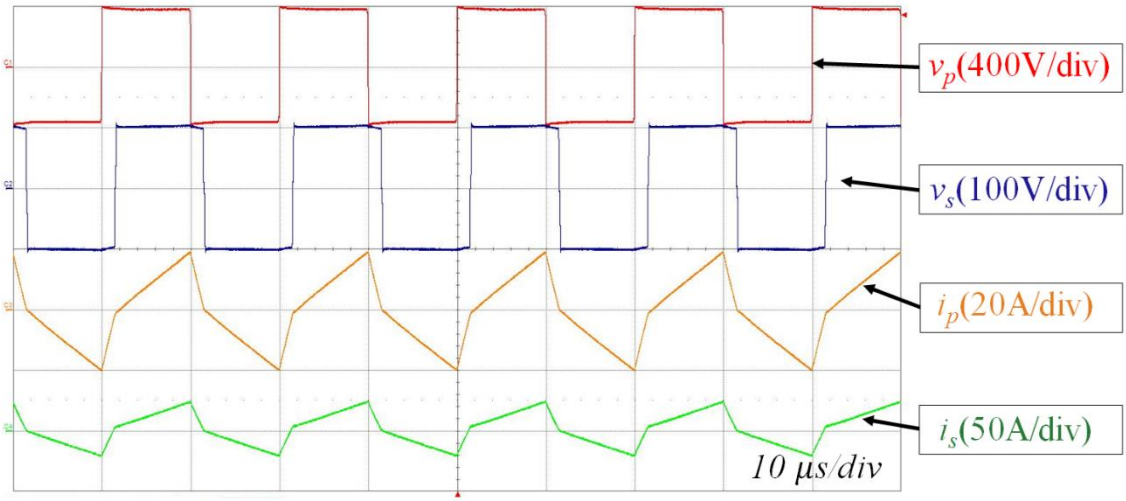


Fig. 3.16 Experimental results of the voltage, current waveforms of primary and secondary side when m=0.4, (a) 1500 W, (b) 1000 W, (c) 500 W



(a)



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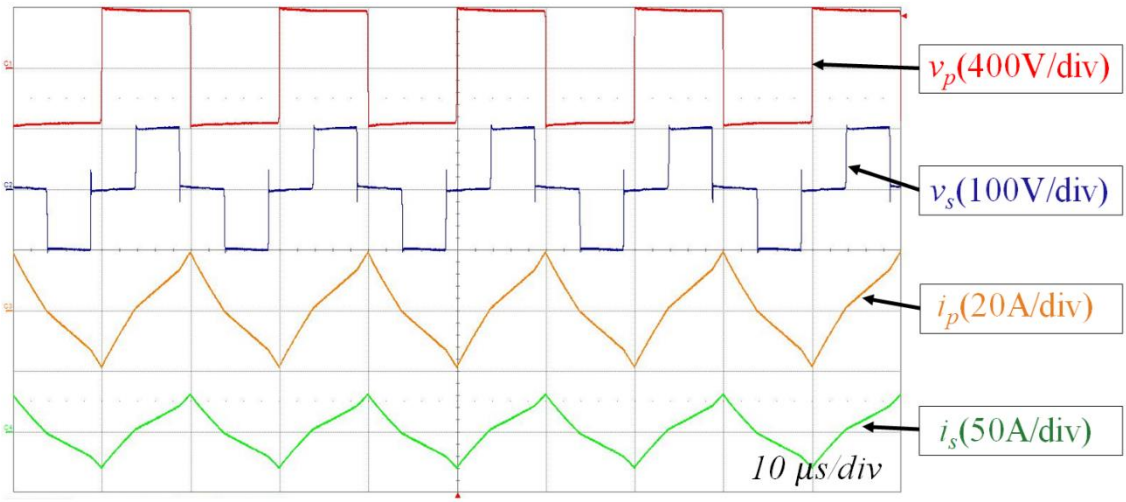
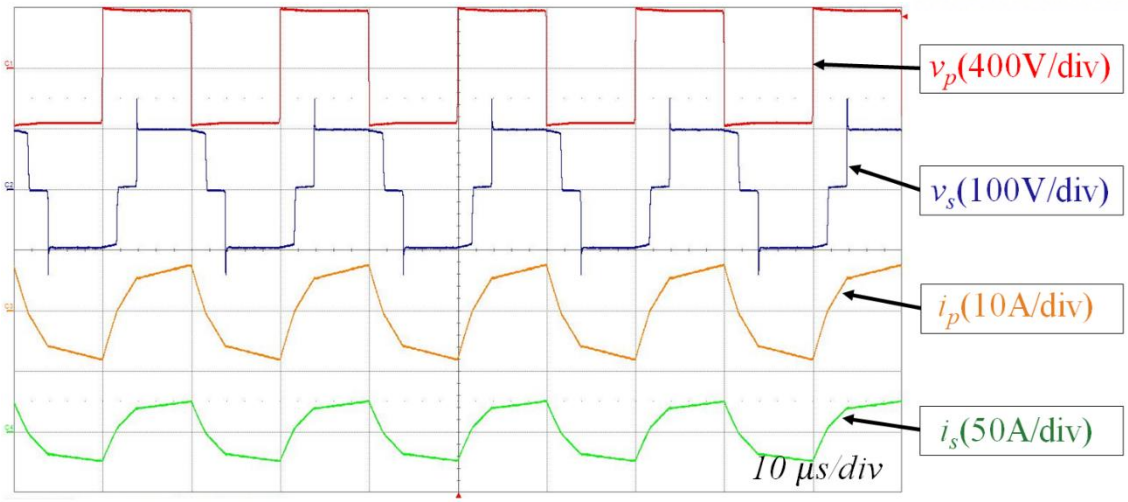
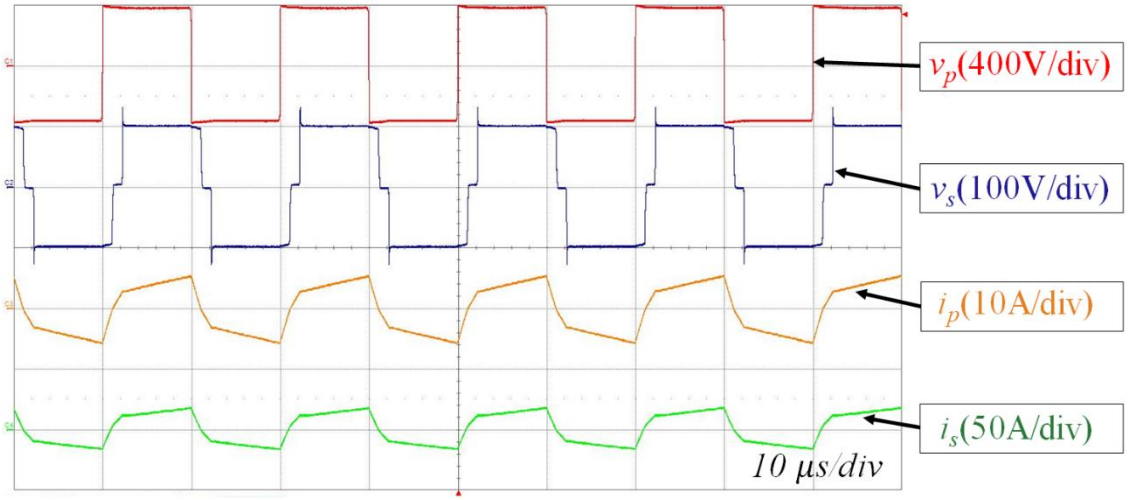


(c)

Fig. 3.17 Experimental results of the voltage, current waveforms of primary and secondary side when m = 0.6, (a) 1500 W, (b) 1000 W, (c) 500 W



(a)



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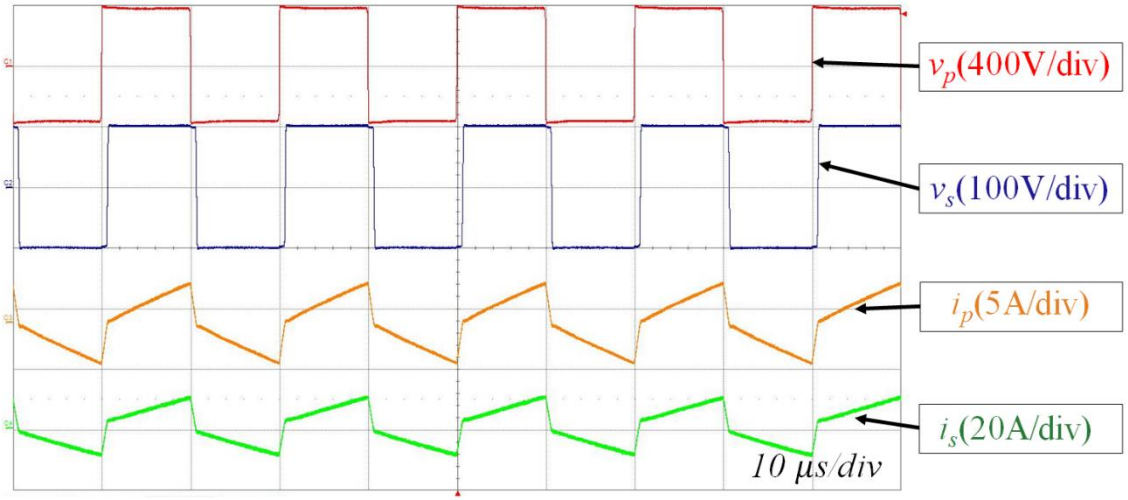
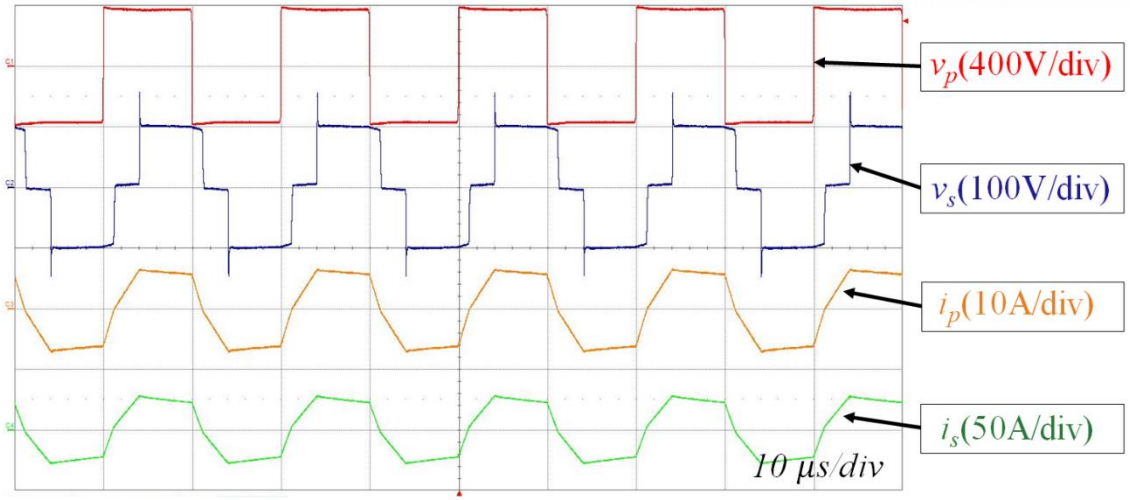
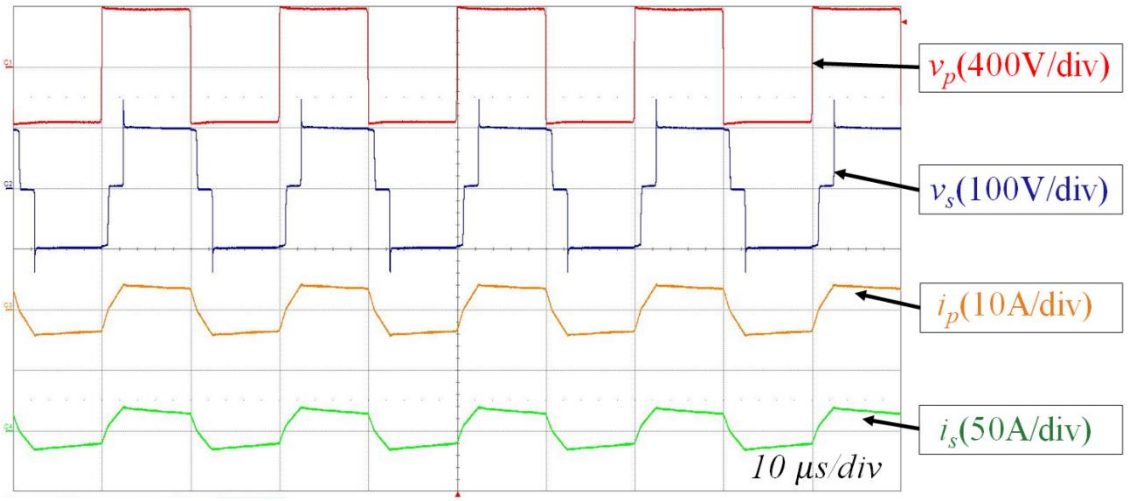


(c)

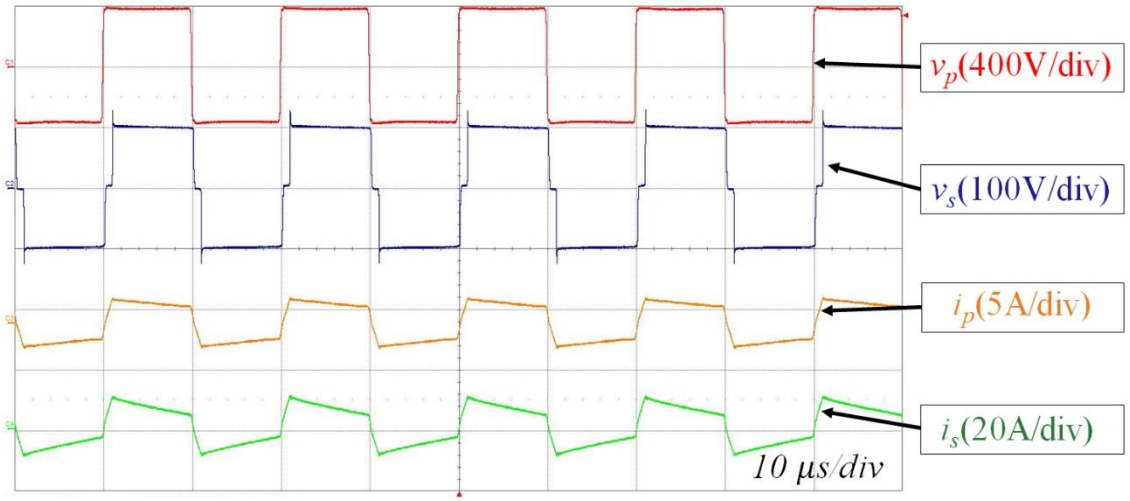
Fig. 3.18 Experimental results of the voltage, current waveforms of primary and secondary side when m = 0.8, (a) 1500 W, (b) 1000 W, (c) 500 W



(a)

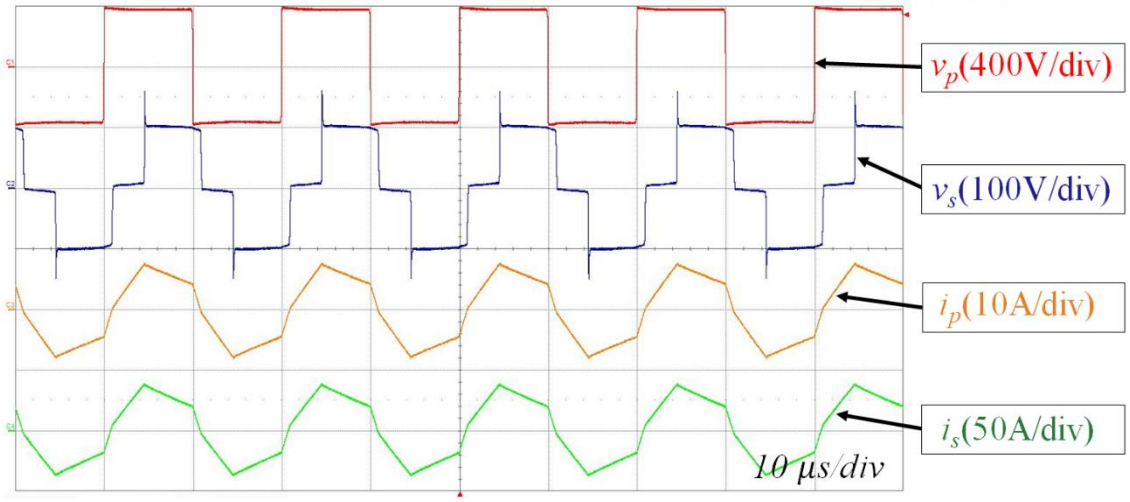


(b)

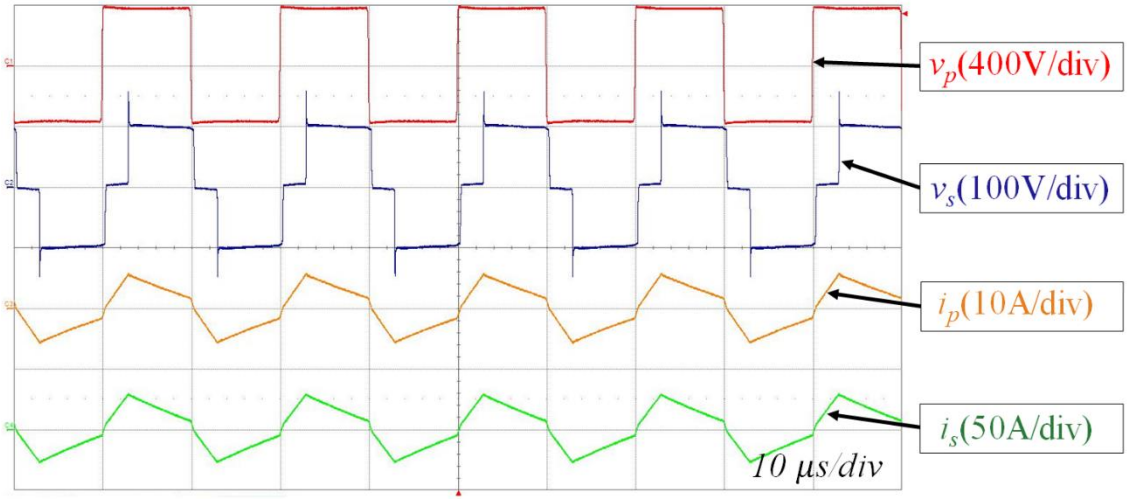


(c)

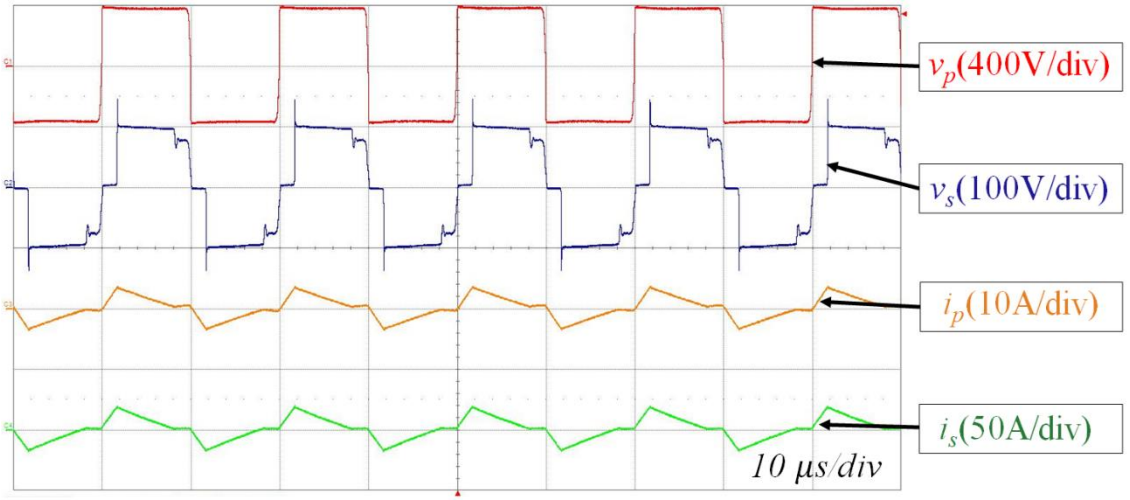
Fig. 3.19 Experimental results of the voltage, current waveforms of primary and secondary side when m = 1, (a) 1500 W, (b) 1000 W, (c) 500 W



(a)



(b)



(c)

Fig. 3.20 Experimental results of the voltage, current waveforms of primary and secondary side when m = 1.2, (a) 1500 W, (b) 1000 W, (c) 500 W

TABLE V EXPERIMENT RESULT OF THE RMS CURRENT OF PRIMARY AND SECONDARY SIDE VARYING VOLTAGE GAIN AT 1500 W, 1000 W, AND 500 W

	1500 W				
	$m = 0.4$	$m = 0.6$	$m = 0.8$	$m = 1$	$m = 1.2$
$i_{p,rms}$	11.13 A	7.665 A	6.123 A	5.411 A	5.282 A
$i_{s,rms}$	17.95 A	17.78 A	19.91 A	21.6 A	25.19 A

	1000 W				
	$m = 0.4$	$m = 0.6$	$m = 0.8$	$m = 1$	$m = 1.2$
$i_{p,rms}$	10.079 A	5.639 A	3.978 A	3.482 A	3.539 A
$i_{s,rms}$	15.9 A	13.27 A	12.74 A	13.76 A	17.1 A

	500 W				
	$m = 0.4$	$m = 0.6$	$m = 0.8$	$m = 1$	$m = 1.2$
$i_{p,rms}$	10.2 A	5.685 A	1.993 A	1.579 A	1.807 A
$i_{s,rms}$	16.14 A	13.10 A	6.09 A	6.46 A	9.14 A

In addition, the primary and secondary rms current values in the figures are summarized in TABLE V. At each load condition, the primary side rms current goes high as the voltage gain decrease from 1 to 0.4. However, because the rms current on the secondary side, $i_{s,rms}$, is multiplied by the rms current on the primary side and the turn ratio of the transformer, n, so the smaller the voltage gain, the smaller the rms current on the secondary side. It should be noted that the value of the rms current on the secondary side is decreasing, although the current waveform is distorted and sharp as the voltage gain moves away from 1. This is because the rms current on the primary side increases in voltage across the series inductor because the voltage magnitude difference between both end of the transformer increases as the turn ratio of the transformer moves away from 1. When the current waveform is inclined, the rms current value and the peak current become large, and the conduction loss generally increases. However, because the turn ratio of the transformer is proportional to the current value on the secondary side, the rms current and peak current on the primary side increase, but it is possible to decrease the rms current and peak current on the secondary side.

TABLE V is the result of numerically organized into RMS current value of the primary side and secondary side of the semi-DAB obtained in the experiment waveforms. Through the values in the TABLE V can be reliably confirm the change in the RMS current values of the primary and secondary sides according to the voltage gain at each load condition, 1500 W, 1000 W, and 500 W. In 1500 W, as the voltage gain goes from 1 to 0.6, the rms current on the primary side ($i_{p,rms}$) is getting bigger from

5.411 A to 7.665 A because the decreased voltage gain (m) makes the current waveform becomes steep. However, because n (turn ratio) become small from 4 to 2.4, the secondary current is reduced from 21.6 A to 17.78 A, which is reduced n (2.4) times increased rms current of primary side (7.665 A). This is because the rms current of primary side increased by 1.41 times, but turn ratio n decreased by 1.66 times, so the secondary current decreased overall. As the voltage gain goes from 0.6 to 0.4, the rms current of the primary side ($i_{p,rms}$) is getting bigger from 7.665 A to 11.13 A because the decreased voltage gain (m) makes the current waveform becomes distort. Although the turn ratio become small from 2.4 to 1.6, the $i_{s,rms}$ increase from 17.78 A to 17.95 A. This is because turn ratio n decreased 1.5 times, but $i_{p,rms}$ increased 1.46 times. So, it was measured almost similarly.

With the same principle, middle-load and light-load condition also can be interpreted. In 1000 W load condition, as the voltage goes down from 1 to 0.8, the primary side rms current increased from 3.482 A to 3.978 A. This is an increase of about 1.14 times. But the voltage gain, m, decreased from 1 to 0.8, that is 1.25 times. Therefore, the decrease is greater than the increment, so overall the current on secondary side ($i_{s,rms}$) is reduced, as provided in TABLE V. The experimental value shows that the secondary RMS current has decreased from 13.76 A to 12.74 A. And as the voltage gain, m, becomes smaller and smaller, the RMS current on secondary side ($i_{s,rms}$) increases because the current increasing amount is bigger than the decreasing amount of the m, according to equation (17). Thus, the secondary RMS current at 1000 W increases as m becomes 0.6 and 0.4.

Lastly, in light-load condition, As the voltage gain went from 1 to 0.8, it is about 1.25 times of decreasing. But, the RMS current of the primary side increases from 1.579 A to 1.993 A. It is 1.26 times increasing. According to equation (17), $i_{s,rms}$ may be 6.316 A, which is 1.579 A times 4. Because the turn ratio is 4 when the voltage gain is unity. When the voltage gain is 0.8, the changed $i_{s,rms}$ may be 6.3 A, which is 1.993 A times 3.2. Because the turn ratio is 3.2 when the voltage gain is 0.8, using the equation (1). So, the experimental result RMS currents of secondary side are almost similarly when m = 1 and m = 0.8. However, in subsequent trends, the increase in the rms current value on the primary side is greater than the decrease in the voltage gain, so the conductivity loss will increase significantly, and efficiency will decrease significantly. Therefore, it is expected to show the best efficiency at m=1 or m = 0.8 under 500 W conditions. These results may vary because the design power rate of the converter or the input and output voltage, or the loss expression of the semi-DAB is determined by the elements used. However, the experiment confirmed that the rms current on the secondary side can be reduced by changing the voltage gain reduced.

As a result of the experiment, it was confirmed that the proposed voltage gain design method showed a similar trend to the previous analysis results. In high-load condition, the smaller the voltage gain value, the greater the rms current value on the primary side ($i_{p,rms}$), but the smaller the voltage gain value, so the rms current on the secondary side ($i_{s,rms}$) tends to decrease rather. It is because the RMS current of the secondary side can be obtained as the product of turn ratio and the RMS current of the primary side.

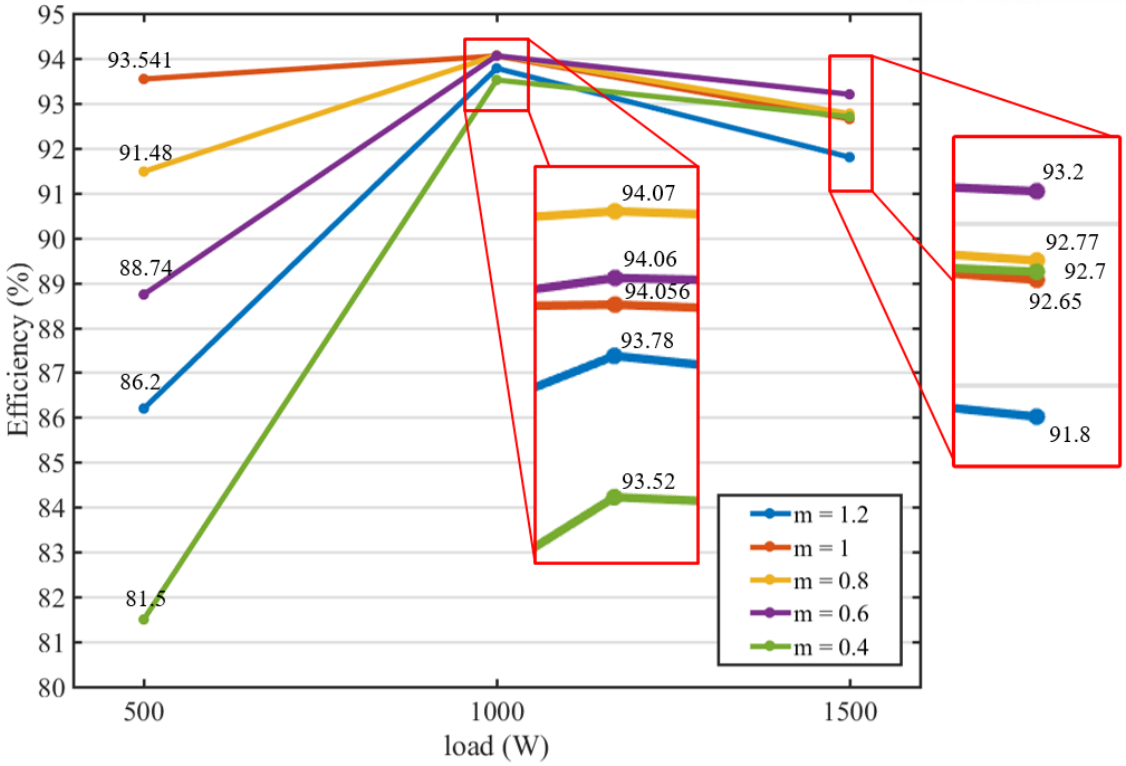


Fig. 3.21 Efficiency curves with varying the voltage gain at 1500 W, 1000 W, 500 W load

In other words, if the reduction in voltage gain is greater than the increase in the primary current, it is possible to reduce the secondary current. The reduction in secondary RMS current results in an increase in efficiency at semi-DAB converter, because the conduction loss on the secondary side is the most dominant.

Thus, the efficiency at each load was measured whether this change in the current waveform led to an increasing the efficiency of the actual semi-DAB converter. The efficiency of the semi-DAB converter was measured by the power analyzer from the N4L. The results of efficiency measurements at each load varying the voltage gain are shown in Fig. 3.5. In full-load, in 1500 W load condition, when the voltage gain m = 0.6 it shows the highest efficiency (93.2 %) due to the smallest conduction loss. This is because the RMS current reduction on the secondary side is much greater than the rms current increase on the primary side, and the conduction loss of the converter is proportional to the square of the rms current, according to (15). And in the middle-load situation (1000 W), it has highest efficiency 94.07 % when the voltage gain is around 0.8. This is because when the voltage gain is less than 0.8, the increment of the primary current is greater than the decrement of m. So, it was experimentally measured that the secondary current increases from 12.74 A to 13.27 A, where the voltage gain changed from 0.8 to 0.6. Therefore, the smaller the gain of m, the lower the efficiency at 1000 W and m = 0.8.

And in light-load 500 W, it shows the best efficiency 93.541 % when the voltage gain is 1. The previous comparison was made between m = 1 and 0.8 at 500 W, and noted that the RMS current on

the secondary side should be almost unchanged, because $i_{s,rms}$ is 6.316 A, which is 1.579 A times four, and the changed $i_{s,rms}$ is 6.3 A, which is 1.993 A times 3.2. However, since the RMS current value on the primary side is the smallest when m = 1, the efficiency at the light load condition is determined by the factors on the primary side rather than the secondary side.

In this section, a voltage gain design method to reducing the conduction loss and increase the efficiency of the semi-DAB converter is proposed. The semi-DAB operation principles and basic current and voltage waveforms are presented, and through simulation and experimental of 1.5-kW semi-DAB converter prototype, the proposed method can be explained and verified. Typically, the voltage gain value is used as a method of reducing the rms of the current, but the optimal voltage gain value is not 1 in applications where the input voltage and output voltage are largely different, such as semi-DAB in the charging application. It is an advantage that the proposed voltage gain design method is proved in an empirical experiment, but the converter does not have a transformer for each load condition, only one transformer must cover with multiple load situations. Therefore, the optimal voltage gain value differs according to the load condition is a limitation of the proposed method. Next chapter, it deals with a method through advanced modulation techniques to improve these limitations of proposed voltage gain design methodology.

IV. ADVANCED MODULATION METHOD

In this chapter, the additional advanced modulation is applied to the proposed voltage gain design method for semi-DAB converter to improve the efficiency. EPS (extended-phase-shift) modulation is a modulation technique proposed to overcome the disadvantage of efficiency in the circulating power generating much in the SPS (single-phase-shift) modulation. As confirmed in the previous chapter, the proposed voltage gain method has a limitation that shows lower efficiency at middle to low loads, it is intended to improve the efficiency using additional modulation, EPS. The validity of the proposed design method is also verified through the simulation, and feasibility can be demonstrated with a 1.5-kW prototype hardware experiment.

4.1 Extended Phase Shift of Semi-DAB

In DAB, there have been researched various modulations existed to achieve different objectives. SPS (single-phase-shift), which was used previous chapter, is the most basic phase-shift switching technique of the DAB. The SPS modulation is not difficult to modulate and control the operation of the simple principle, it can transfer the power [32]. As mentioned before, in SPS modulation, the two switches of primary side H-bridge located diagonally (S_{p1}–S_{p4}, S_{p2}–S_{p3}) in Fig. 4.1 are switched on and off in pairs simultaneously [33]-[35]. SPS modulation is preferred because it is easy to implement, but there is a serious disadvantage that circulating power exists because there is a region where reactive power occurs. Fig. 4.1 shows the principle for the reactive power and circulating power generated in the SPS modulation in semi-DAB to the waveform. In the period where the reactive power is generated, the voltage is positive when the i_p has negative current and a reactive power is generated. In addition, the interval in which the reactive power occurs exists twice in one period. Therefore, the circulating power in SPS has the effect of significantly reducing the efficiency of the converter.

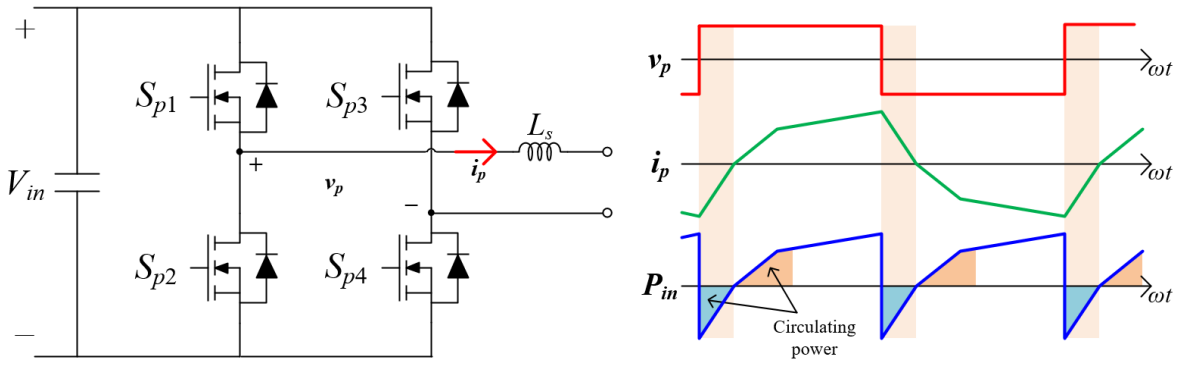


Fig. 4.1 Conceptual diagram of reactive power and circulating power generation in SPS modulation

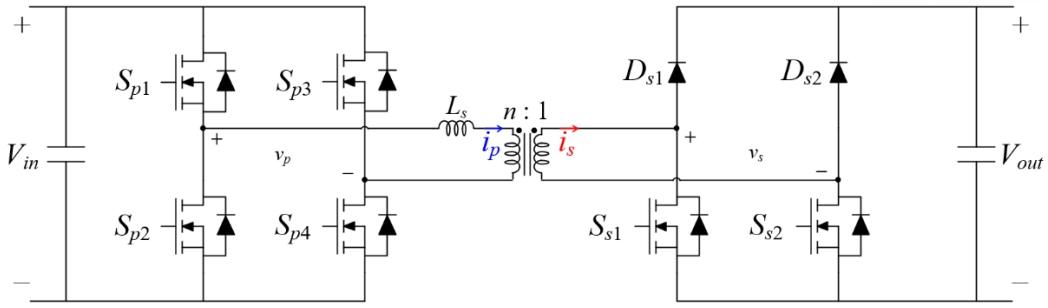


Fig. 4.2 Converter schematics : The semi-dual-active-bridge (semi-DAB)

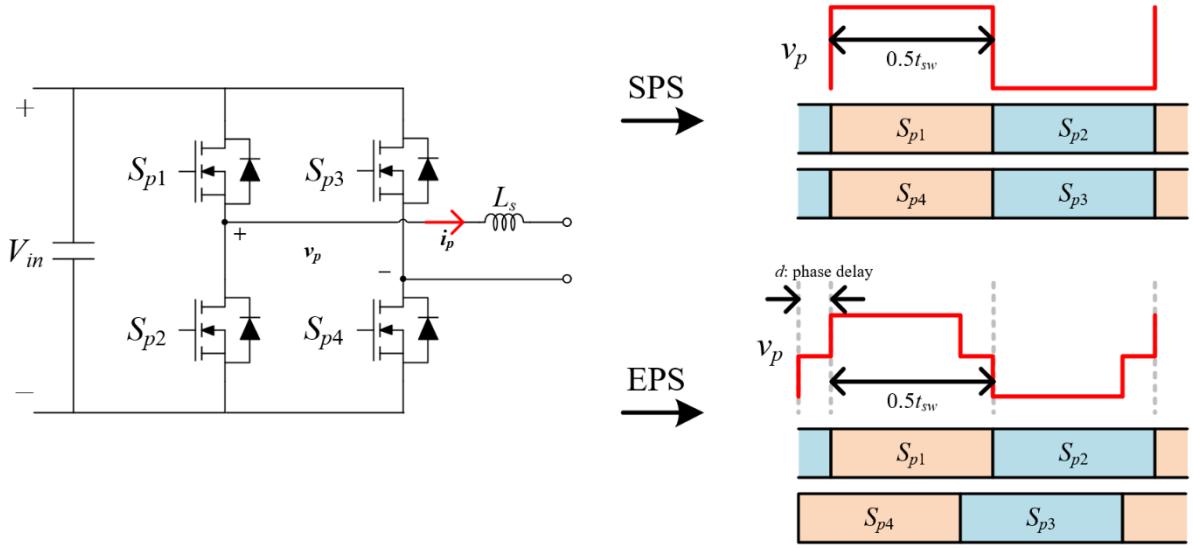


Fig. 4.3 Switching modulation principle and voltage waveform of primary side of SPS and EPS

The circuit schematic of the semi-DAB is shown in Fig. 4.2 given with the current, voltage and the notation of each elements. The switches of S_{p1}, S_{p2}, S_{p3}, and S_{p4} are the switches in primary side of semi-DAB, and S_{s1}, S_{s2} are the switches in secondary side of semi-DAB. And D_{s1}, D_{s2} presents are the diodes in secondary of semi-DAB converter. The EPS stands for modulation of the primary switches. Fig. 4.3 shows the switching principle and conceptual waveform of voltage of the primary side. The Fig. 4.3 shows the differences between SPS and EPS modulation. In SPS, diagonally positioned switches, S_{p1} and S_{p4}, S_{p2} and S_{p3}, always operate in pairs with 50 % duty, whereas the EPS has a phase delay between the diagonally positioned switches. The switches on EPS also operate with 50 % duty. Then, the phase delay between S_{p1} and S_{p4} produces a zero voltage at the primary side of the semi-DAB. These zero voltages eliminate the positive voltage of the reactive power section produced in the semi-DAB, resulting in a reduction in the circulating power.

The comparison with modulation operating waveforms between SPS and EPS is illustrated on Fig. 4.4. Fig. 4.4 (a) shows an SPS modulation operation, and Fig. 4.4 (b) shows an EPS modulation operating process. In SPS, S_{p1}–S_{p4} and S_{p2}–S_{p3} can be seen that each operate at the same time, but the

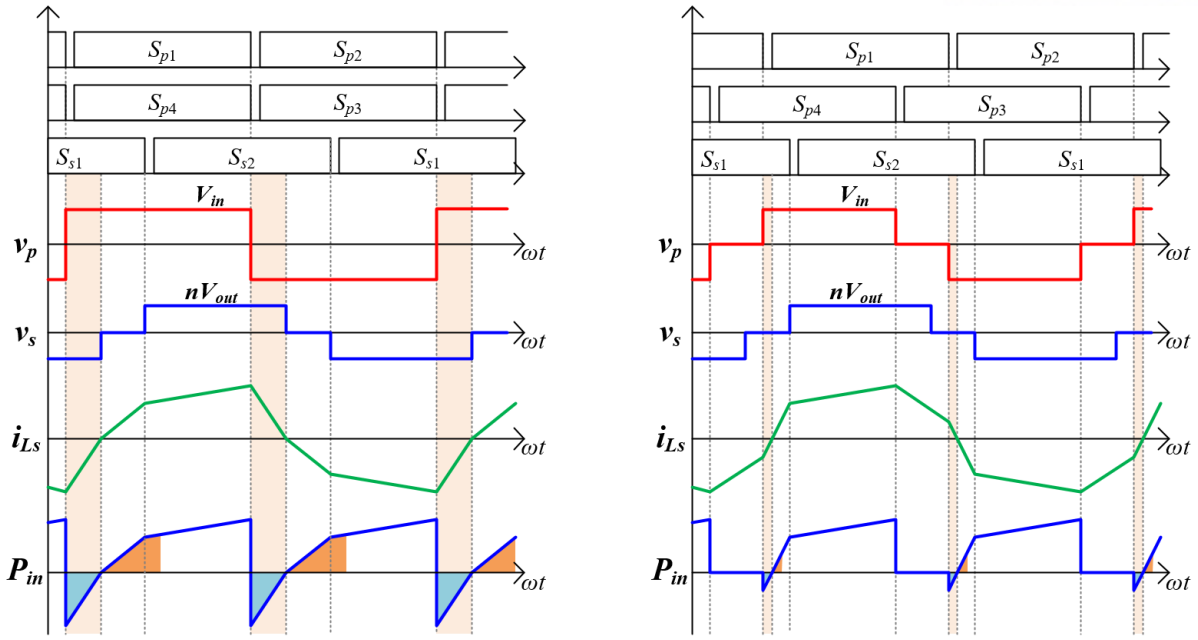


Fig. 4.4 Comparison with modulation operating waveforms between (a) SPS and (b) EPS

EPS, S_{p1}–S_{p4} and S_{p2}–S_{p3} can be seen that has some phase delay. Therefore, in SPS, the voltage waveform on the primary side (v_p) appears the same as the normal square-wave, but in EPS, it can be seen by the waveform that the zero voltage interval occurs. In the waveform of the input power in each modulation mode, light blue and orange regions are displayed in the circulating power generation. Since reactive power is generated in a section in which the current direction on the primary side and the voltage on the primary side are opposite, the same amount of real power has to eliminate the reactive power. After that, the reactive power generated can be eliminated with the same amount of effective power and only the remaining power can be transferred to the secondary side.

And from Fig. 4.4, there is a change in the shape of the current waveforms between the SPS and EPS modulation. The reason why the waveform of the current flowing to the transformer at SPS and EPS is different is that the voltage waveform on the transformer changes as the zero voltage section occurs on the primary side. Comparing Fig. 4.4 (a) and (b), it can be seen that the circulating power is significantly reduced in the EPS modulation compared to the SPS modulation.

The operating principle process in semi-DAB topology is shown as Fig. 4.5. The operating principle process of the semi-DAB consists of a total of 8 circuit operations (a)–(h). The circuit principle of EPS is more complex because of the addition of the zero voltage section on the primary side compared to the circuit principle at SPS. The zero-voltage section in semi-DAB with EPS modulation can be seen in Fig. 4.5 (a), (b), (e) and (f). In this period, it prevents the reactive power is unnecessarily consumed because even if the current flows to the transformer takes the input voltage opposite. Therefore, the

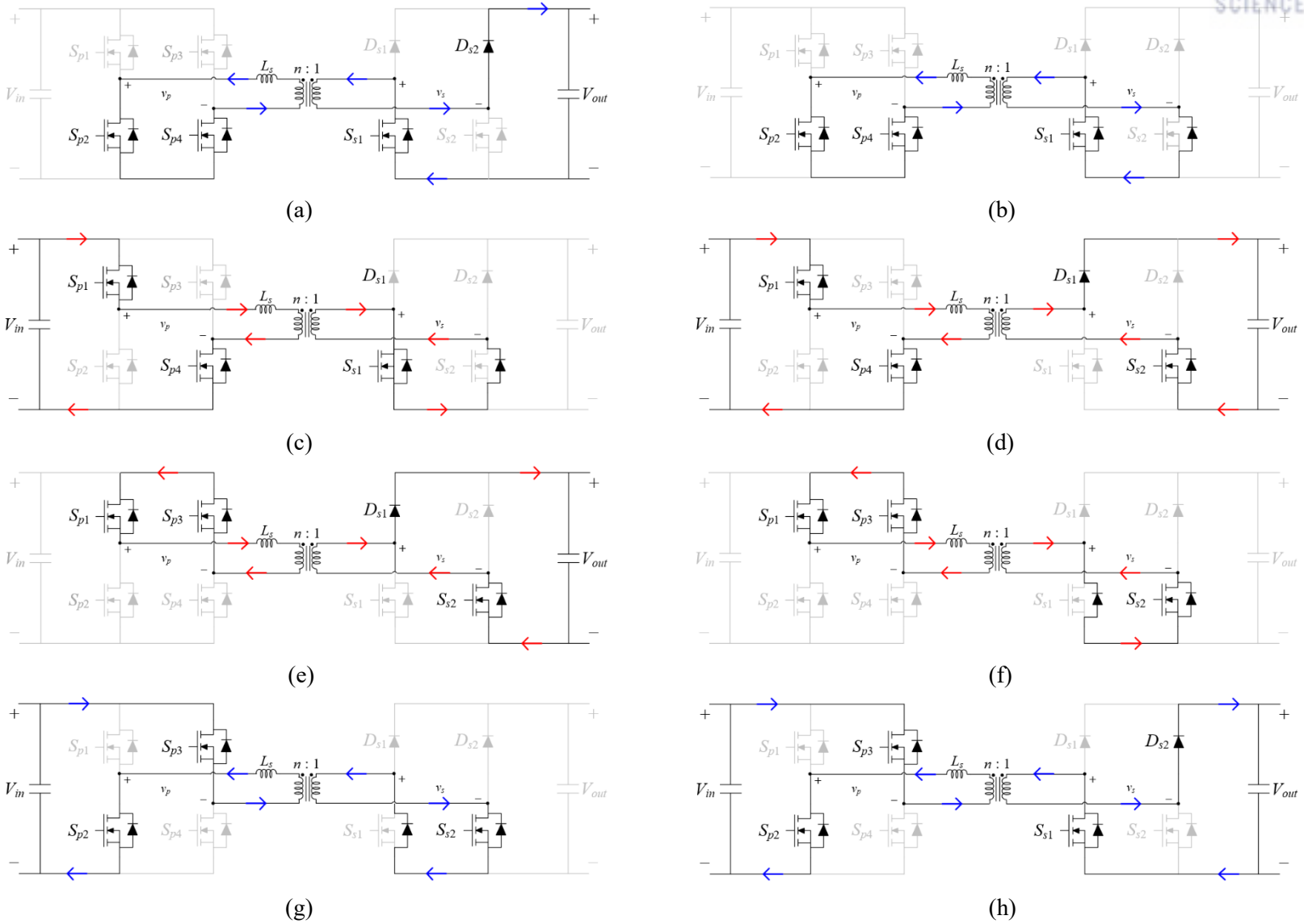


Fig. 4.5 Operating principle and process in semi-DAB

TABLE VI THE SYSTEM SPECIFICATIONS AND PARAMETERS USED FOR SIMULATION OF THE EPS MODULATION IN SEMI-DAB

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Output voltage	V_{out}	95 V
Turn ratio	n:1	2.4
Voltage gain	m	0.6
Rated power	-	500 W, 1000 W, 1500 W
Power inductor	L_m	120.96 μH
Switching frequency	f_{sw}	50 kHz

power delivered through EPS in DAB can be obtained by the following equation [29],

$$P = \frac{nV_{in}V_{out}}{2f_{sw}L_s}[D_2(1-D_2) + \frac{1}{2}D_1(1-D_1-2D_2)] \quad (22)$$

, where the D_1 is inner phase shift that cause between the S_{p1} and S_{p4}, and D_2 is the outer phase shift between the primary and secondary side voltages. The D_2 in this equation has the same meaning as ϕ in SPS modulation. When used in combination of (22) and (10), the transferred power in semi-DAB can be derived.

In the following section, simulations are performed to find out how the voltage and current waveforms of each port are formed when EPS is applied, and to set the magnitude for the phase delay for experimentation, rather than when SPS is applied to semi-DAB.

4.2 Simulation Results

To verify a further efficiency improvement in the additional EPS modulation with the voltage gain optimal value, a 1.5-kW semi-DAB converter prototype was implemented through simulation. The simulation was performed using PSIM simulator. Based on the parameters and system specifications are listed in TABLE VI. The power rate of the semi-DAB was implemented in 1.5-kW scale, input voltage is 380 V, and output voltage is set to 95 V, as same with previous converter. And turn ratio of the transformer for semi-DAB is set to 2.4, so the voltage gain is set to 0.6. This is because in the previous chapter, m=0.6 was optimized for the voltage gain with the highest efficiency at full-load while minimizing the conduction loss of semi-DAB converter. Therefore, at the optimized voltage gain obtained based on full-load condition, it will be shown whether a further efficiency improvement is possible through EPS modulation. So, the power inductor under the conditions in TABLE VI was determined by using 120.96 μH optimal inductance to obtain an equation of the semi-DAB. And the

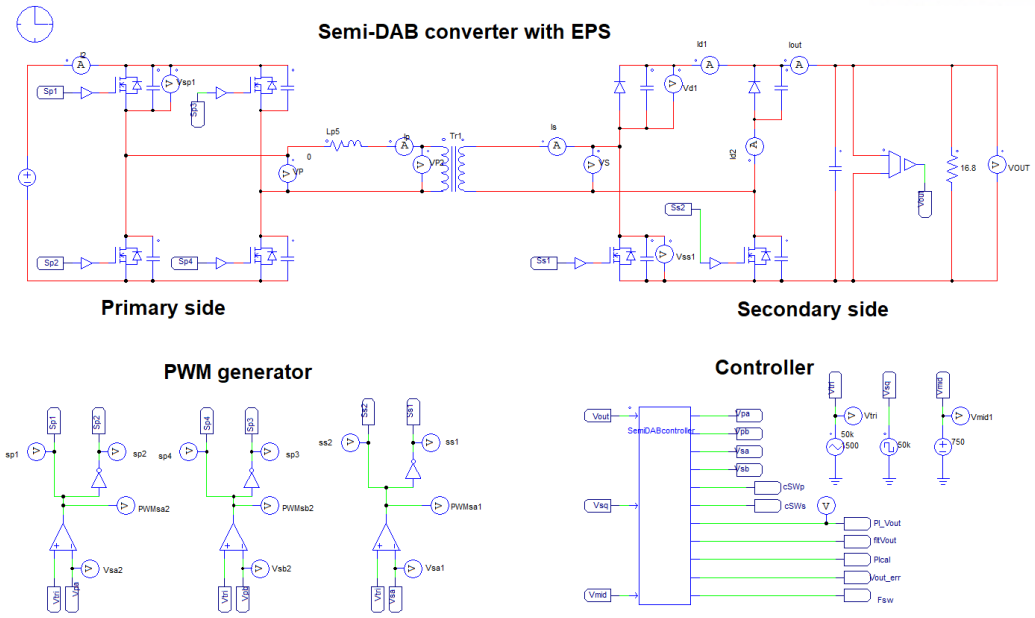
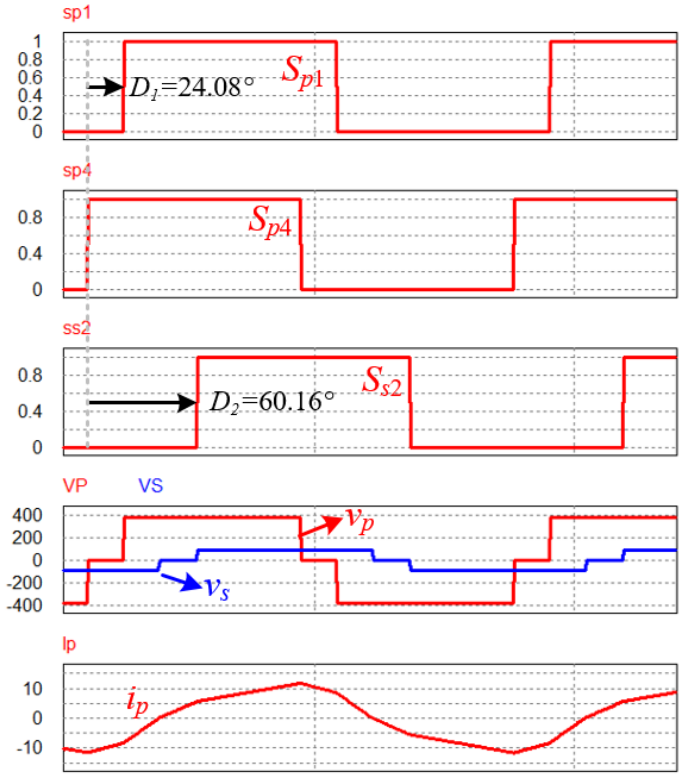


Fig. 4.6 The semi-DAB converter with EPS modulation implemented in PSIM

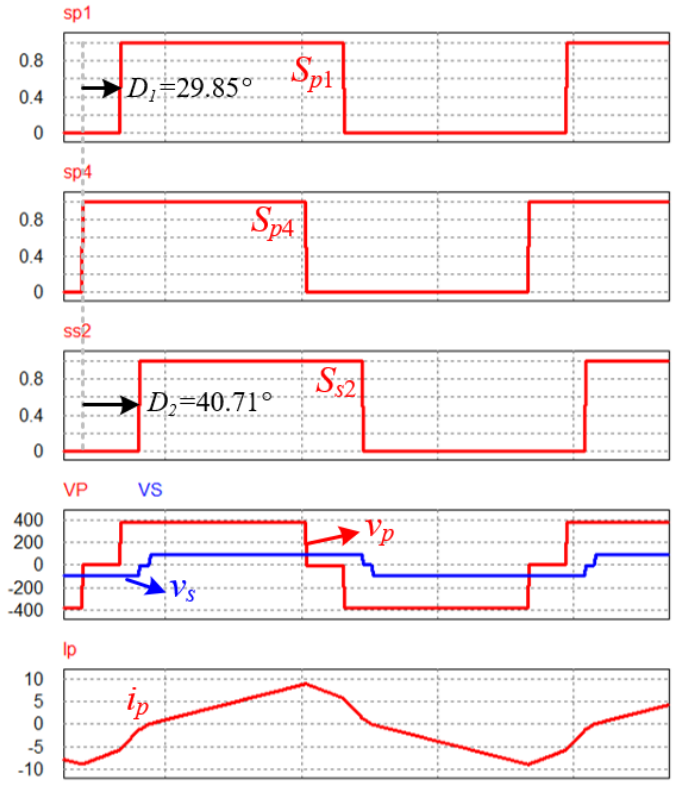
switching frequency of the designed converter is set to 50 kHz. This is the switch frequency set at high speed to increase the power density of semi-DAB converter. Increasing the switching frequency of the converter, it is possible to reduce the size of the transformer and inductor, magnetizing elements, as it takes the effect of increasing the power density of the entire converter, it is to be preferred to use a high-switching frequency. And each of the high-load, middle-load, and light-load condition, loads of 1500 W, 1000 W, and 500 W conditions were simulated.

Fig. 4.6 is the semi-DAB converter with EPS modulation circuit implemented using PSIM. There are existed in semi-DAB with EPS modulation power stage circuit including primary side and secondary side, PWM generator, and controller. The designed semi-DAB controller is implemented as a C-block because it will use a digital controller. As shown in Fig. 4.6, the primary side H-bridge consist of 4 switches, and secondary side H-bridge have 2 diodes and 2 switches. And between them, series power inductor and transformers are connecting. The load of 1500 W, 1000 W, and 500 W are implemented as a resistance of 6 Ω, 9 Ω, and 18 Ω in simulation. In addition, the parasitic components, output capacitance or on-resistance of switches, and the values provided in the datasheet of each device were used for the switches and diodes used in the semi-DAB converter simulation. The switch referred to the datasheet in STW48N60DM2 from STMicroelectronics, and the diode referred to the datasheet in DSEP29-60A from IXYS.

The results of the simulation waveforms are shown in Fig. 4.7. In Fig. 4.7 (a) shows the voltage and current waveforms with voltage gain m=0.6 at 1500 W, Fig. 4.7 (b) depicts the waveforms in case of m=0.6 in 1000 W load condition, and Fig. 4.7 (c) shows that the results of the waveforms when the voltage gain is 0.6 in 500 W load condition. In the circuit operation in the semi-DAB, there is an inner



(a)



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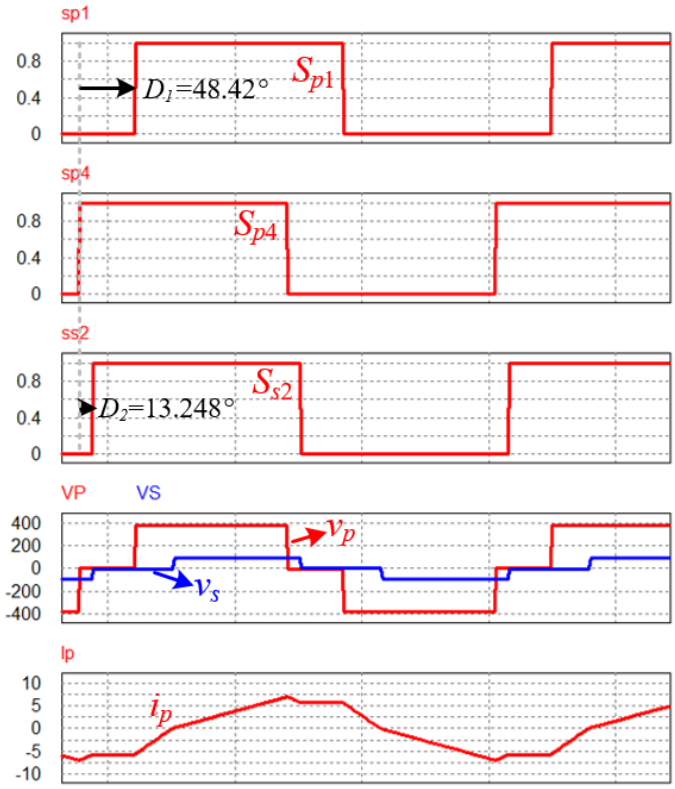


(c)

Fig. 4.7 The simulation results of the switching pattern, voltage and current waveforms with voltage gain m=0.6 at (a) 1500 W, (b) 1000 W, (c) 500 W

phase shift D_1 and an outer phase shift D_2, as mentioned in previous chapter 4.1. The D1 is the inner-phase-shift between the driving signals of S_{p1} and S_{p4} in the primary side of the semi-DAB, and D_2 is the outer-phase-shift, which is the phase shift ratio between the primary and secondary side voltages of the semi-DAB converter. In 1500 W load condition, the outer phase shift D_2 is 60.16º and the inner phase shift D_1 is set to 24.08º, as shown in Fig. 4.7 (a). And in the voltage waveform of primary side, a zero voltage interval due to EPS modulation is observed. In 1000 W load, the outer phase shift D_2 is 40.71º and the inner phase shift D_1 is set to 24.34º, as shown in Fig. 4.7 (a). D_2 is reduced because the transmission power at 1000 W is reduced, compared to 1500 W. In addition, in the primary-side voltage waveform, the zero voltage was found to exist in the negative-current interval of the primary side, thus reducing the circulating power is expected to be reduced. The waveforms at 500 W is shown in Fig. 4.7 (c). In 500 W load, the outer phase shift D_2 is 13.248º and the inner phase shift D_1 is set to 48.42º. Because the output power was reduced to 500 W, the phase difference between the primary side and secondary side, as same with D_2, was reduced. However, D_1, which determines the region of the zero-voltage interval from the primary voltage, is considered to have increased, and the circulating power is reduced the most at 500 W, so a large increase in efficiency in expected.

TABLE VII SIMULATION RESULT OF THE RMS CURRENT OF PRIMARY SIDE AT THE VOLTAGE GAIN 0.6 WITH VARYIHNG 1500 W, 1000 W, AND 500 W

	$m = 0.6$		
	1500 W	1000 W	500 W
SPS	7.82 A	5.78 A	5.63 A
EPS	7.7 A	5.42 A	4.479 A

TABLE VII shows that the simulation results of RMS current of the primary side at the voltage gain is 0.6 with varying the load-condition, 1500 W, 1000 W, and 500 W. From this simulation result, it is possible to predict the change in efficiency of semi-DAB before and after applying the EPS modulation. When the voltage gain was 0.6 and the load was 1500 W, the simulation result of the primary side RMS current of semi-DAB through SPS was 7.82 A, but it was reduced to 7.7 A when EPS was applied. So, under the full load, it is expected the change in the efficiency of semi-DAB will not be significant due to the application of SPS and EPS. And the load was 1000 W, the RMS current of primary side is reduced from 5.78 A to 5.42 A, after changing the modulation from SPS to EPS. There will be a slight increase in efficiency since the change in current is larger than when it is 1500 W. Finally, the simulation results show that at 500 W, under light-load condition, the primary current at SPS is from 5.63 A to 4.479 A after EPS application. Since the value of the RMS current on primary side is dramatically reduced than in the case of heavy load or middle load, a large increase in semi-DAB efficiency at light-load is expected.

4.3 Experimental Results

To verify feasibility of that the additional modulation EPS applied to the proposed voltage gain design method can increase the efficiency of the semi-DAB converter, a 1.5-kW prototype hardware was modified. The produced 1.5-kW hardware prototype is depicted in Fig. 4.8. The hardware includes primary-side and secondary-side board. In prototype hardware board uses fast-recovery MOSFETS, STW48N60DM2 from STMicroelectronics, and fast-recovery diodes, DSEP60-12A from IXYS. And digital controller DSP, TMS320F28335 from Texas Instruments, is used as controller. The EPS modulation was implemented through DSP. The ferrite cores are used in power inductor and transformer, which is EER6062S manufactured by Samhwa Electronics. And using the voltage sensor, sensing the output voltage to control the output voltage of the converter.

The specification of the prototype hardware for experiment are listed in TABLE VIII. The input voltage is set to 380 V, and output voltage is set to 95 V, because 380 V is the standard voltage for DC distribution, and 95 V is set four times lower than the input voltage. And the transformer and inductor was manufactured by matching the optimal transformer turn ratio and voltage gain, since the voltage

TABLE VIII THE SYSTEM SPECIFICATIONS AND PARAMETERS USED FOR 1.5-kW PROTOTYPE OF THE EXPERIMENT WITH EPS MODULATION IN SEMI-DAB

Parameter	Symbol	Value
Input voltage	V_{in}	380 V
Output voltage	V_{out}	95 V
Turn ratio	n:1	2.5
Voltage gain	m	0.625
Rated power	-	500 W, 1000 W, 1500 W
Power inductor	L_m	110.8 μH
Switching frequency	f_{sw}	50 kHz

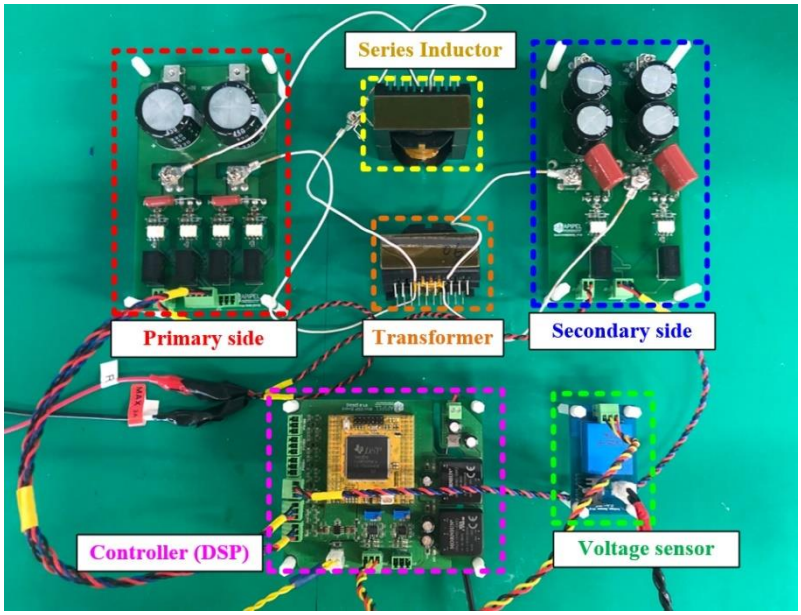
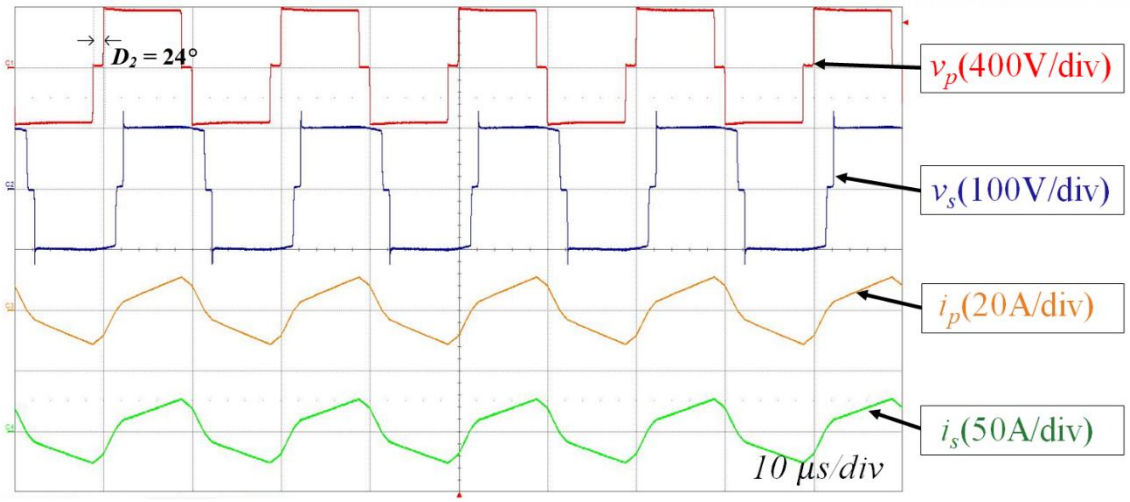


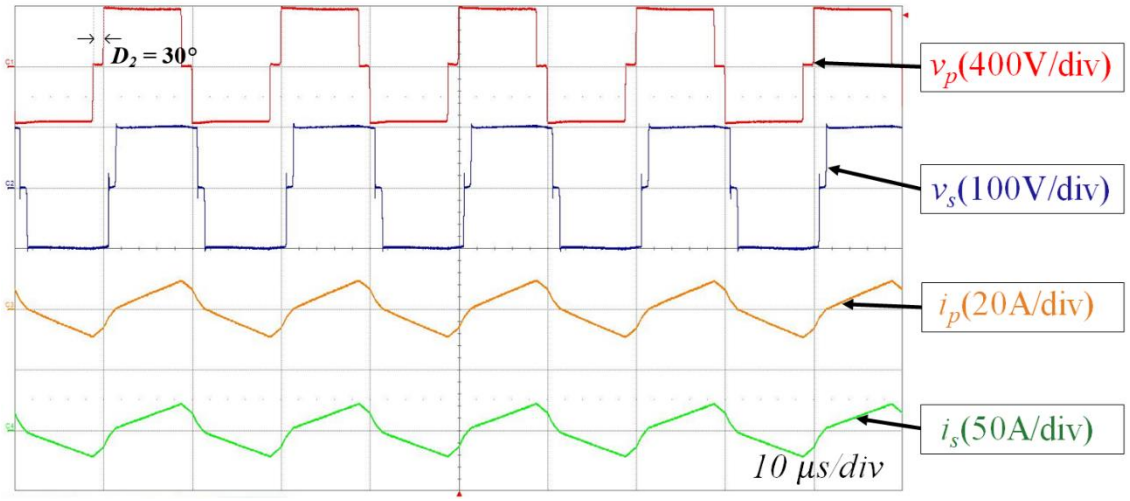
Fig. 4.8 1.5-kW semi-DAB converter prototype and experimental environment

gain optimized was 0.6 in previous chapter. And the load of 1500 W, 1000 W and 500 W were consisting of passive load resistor. Each 1500 W, 1000 W and 500 W represented for full-load, middle load, and light load conditions.

The Fig. 4.9 shows the experimental result waveforms with various load conditions at voltage gain setting to 0.6 under the EPS modulation. Since EPS modulation is applied, it can be confirmed that the zero voltage section is present at the primary side voltage waveform (v_p) in the experiment waveform. In each load condition, the inner-phase-shift which determines the size of the zero voltage section in primary side voltage value was given differently. In 1500 W condition, inner phase 24 º of is given, inner phase 30º is given in 1000 W condition, and inner phase 48 º is given. It can be confirmed from the waveforms that the zero voltage section is formed as much as the inner-phase-shift is given.



(a)



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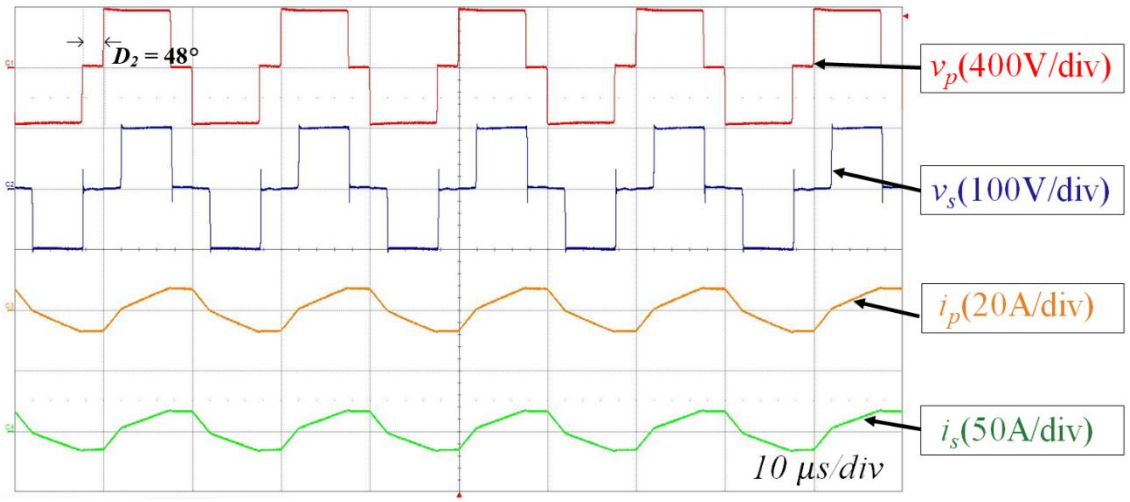

(c)

Fig. 4.9 Experimental results of the voltage, current waveforms of primary and secondary side applied to EPS modulation when m = 0.6, (a) 1500 W, (b) 1000 W, (c) 500 W

TABLE IX COMPARISON EXPERIMENT RESULT OF THE RMS CURRENT OF PRIMARY AND SECONDARY SIDE AT THE VOLTAGE GAIN 0.6 WITH EPS MODULATION

$i_{p,rms}$	m = 0.6		
	1500 W	1000 W	500 W
SPS	7.665 A	5.639 A	5.685 A
EPS	7.175 A	5.32 A	5.07 A

$i_{s,rms}$	m = 0.6		
	1500 W	1000 W	500 W
SPS	17.78 A	13.27 A	13.1 A
EPS	17.42 A	12.98 A	11.79 A

The RMS current of the primary and secondary sides obtained as a result of the experiment are summarized in TABLE IX for each modulation operation, SPS and EPS. Therefore, it is possible to identify the change in the RMS current for each load conditions in each modulation operation. It can be seen that in all the load conditions, the value of the RMS current is decreased in both the primary and secondary sides in EPS modulation than in the case of SPS. In particular, the reduction was greatest at low loads. In the full-load condition, the primary RMS current is 0.5 A, secondary side is 0.4 A reduced. On the other hand, under the light-load 500 W condition, RMS current on the primary side decreased by 0.68 A and on the secondary side by a 1.3 A decreased. This is notable for RMS current reduction on the secondary side, especially since the optimized voltage gain under light load condition showed worse efficiency than m = 1. Therefore, it shows that EPS modulation can complement weakness in the proposed voltage gain design method in SPS, thus increasing efficiency of the semi-DAB converter even under middle-to-light load condition.

The Fig. 4.10 presents the efficiency curves of the semi-DAB applied to SPS and EPS according to power variations. The power variations of the efficiency curves are 1500 W, 1000 W, and 500 W. The EPS modulation shows high efficiency than SPS modulation in middle load. And in 500 W load condition, it shows much higher efficiency than SPS, either. Rather, the rate of increase is the lowest at high loads, and the rate of increase is high at light load. It seems that the efficiency increased because the zero voltage section became larger as the load went higher and the circulating power decreased .Therefore, it can be confirmed from the TABLE IX and the efficiency figure that the RMS current on each side also increased because the circulating power decreased. Therefore, when considering the overall efficiency, it can be seen that the semi-DAB converter applying the EPS modulation and voltage gain design method has the best efficiency.

The conduction loss between SPS and EPS modulation at each load are estimated and shown in Fig. 4.11. This is because the increase in the efficiency of the semi-DAB comes from the conduction loss of

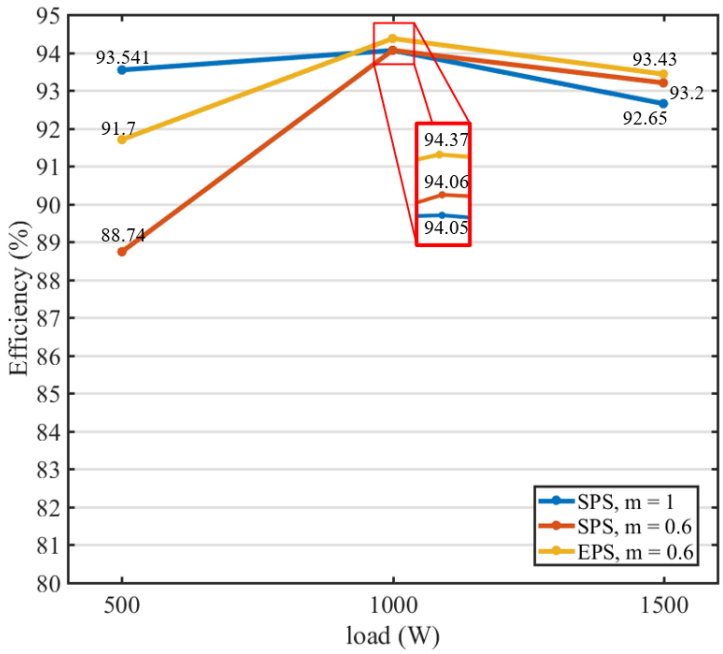

Fig. 4.10 Efficiency curves with varying modulation SPS and EPS at 1500 W, 1000 W, 500 W load

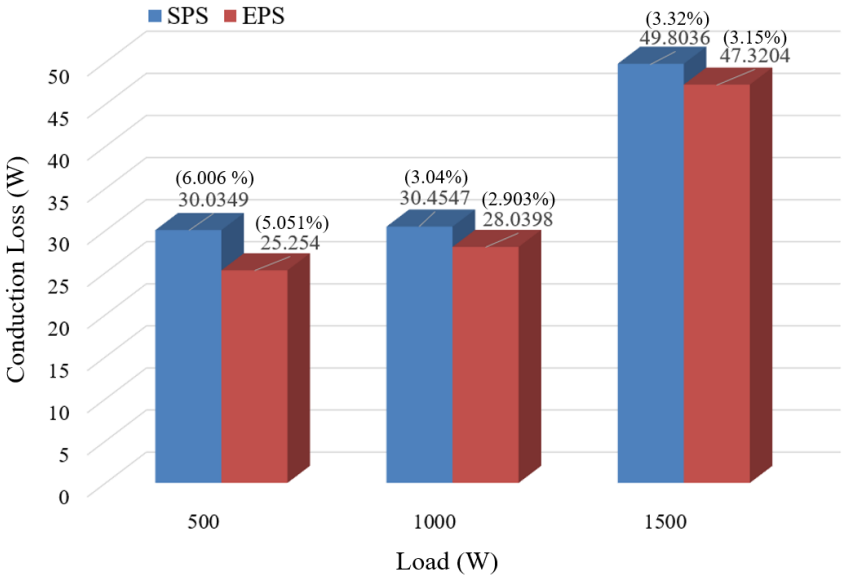

Fig. 4.11 Estimated Loss comparison between SPS and EPS at 1500 W, 1000 W, and 500 W load

the converter. In 1500 W load condition, the estimated conduction loss difference is 2.48 W. It is 0.2 % difference in efficiency. It can be confirmed in Fig. 4.10. And under the 1000 W condition, the estimated conduction loss difference is about 2.4 W. When converted to efficiency, it shows an increase in efficiency of about 0.1 %. Lastly, in 500 W load condition, the reduced conduction loss is 4.7 W, shown in Fig. 4.11. That means an increase of about 1 % of efficiency. However, the efficiency graph shows that there is an increase in efficiency of about 2.4 % in 500 W, so the remaining 1.4 % is expected to decrease in other factors. Under the light-load conditions, the proportion of the conduction loss in the

total loss is not dominant, so it can be assumed that there will also be a reduction in the loss of switching loss or magnetic components. At light load to the application of the EPS modulation seen to have decreased RMS current of the primary side and secondary side is, because also been lowered value of the average current of the switching loss it is also be lowered. In addition, the peak current is also decreased so the loss of the inductor winding loss and transformer loss are also predicted to decreased. So, the effect of the EPS has resulted in a great increase in efficiency at light load of semi-DAB. Therefore, through the experiment, efficiency under high load at the optimized voltage gain value using proposed voltage gain design method through the application of modulation EPS also confirmed the feasibility that can be greatly improved.

In this chapter, the EPS modulation was applied to the reinforcement proposed methodology of a voltage gain design in the semi-DAB. The basic concept and principle of EPS modulation and the operation process of semi-DAB applied with EPS are explained. The effects that can be expected when EPS modulation is applied, increased efficiency due to reduction of circulating power, were analyzed and simulated. As a result of the experiment, the change in the RMS current and the change in efficiency at the optimal voltage gain value when SPS and EPS are applied are shown as experiments. By applying EPS, it showed an efficiency of up to 93.43 % at high load and 91.7 % at low load, but this is an increase in efficiency of about 3 %. Therefore, through the 1.5-kW semi-DAB prototype experiment, it was shown that the voltage gain design method presented under the middle-low load can be supplemented by additional EPS modulation.

V. CONCLUSION

In this thesis, the advanced voltage gain design methodology of transformers was proposed that can improve the efficiency of semi-DAB. First, through the loss analysis of the semi-DAB in the charging applications, it was found that the dominant cause of the loss is the conduction loss of the secondary side of the semi-DAB. Therefore, as a method to reduce the conduction loss of the semi-DAB on the secondary side, a voltage gain design method was proposed through distortion of the transformer turn ratio of the semi-DAB converter. And the concept and principle of the proposed design methodology were explained, and the equations of the optimized voltage gain *m* were obtained through the proposed design method. So, the optimized voltage gain value was intended to optimize the voltage gain that has the lowest conduction loss by considering both the increased primary side RMS current and the decreased secondary side RMS current. Through the analysis of the current equation of the semi-DAB, the value of the most accurate optimal voltage gain was found by MATLAB, 0.5382 in 1500 W. The effectiveness and validity of the proposed design method was also verified by simulation, and feasibility was demonstrated with a 1.5-kW prototype hardware experiment.

And additional advanced EPS modulation is also applied to improve the efficiency of the semi-DAB converter under the various load condition. There is a limitation that the voltage gain method can show lower efficiency than other voltage gain at middle-to-light load conditions. Therefore, EPS modulation, which is a switching modulation method that can increase efficiency by reducing the circulating power of semi-DAB under the middle and light load, has been applied to overcome the limitations of the voltage gain design method. And the feasibility of the proposed voltage gain design method applied to EPS has been demonstrated with simulation and a 1.5-kW prototype of semi-DAB experiments. The experimental results denote that the proposed voltage gain design method confirmed that the efficiency at the light load of the optimized voltage gain can be further improved through additional EPS modulation.

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APPENDIX

A. Derivation of i_{L0} and i_{L1} of inductor current of the semi-DAB

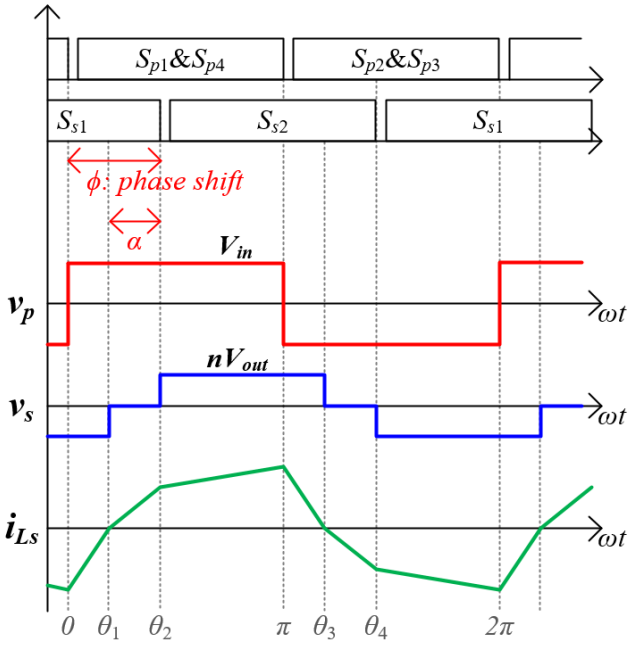

Fig. A1. The voltage and current waveform of semi-DAB converter when the voltage gain $m < 1$

Fig. A1 shows that the voltage and current waveforms of semi-DAB converter. The voltage gain value does not matter to obtain the current equation of the semi-DAB, but for example, $m < 1$ case was shown. Using equation (3), (4), and (5), the current value at each transition interval can be obtained. The current values at each transition interval are expressed by i_{L0} and i_{L1}. In addition, the current waveform is symmetric opposite per π. So, $i(0) = -i(\pi) = -i_{L0}$, $i(\theta_1) = i(\theta_3) = 0$, and $i(\theta_2) = -i(\theta_4) = i_{L1}$ can be established. Then, i_{L0} and i_{L1} is as below:

$$i_{L0} = \frac{V_{in}+nV_{out}}{wL}(\phi - \alpha) \tag{A1}$$

$$i_{L1} = \frac{V_{in}}{wL}\alpha \tag{A2}$$

In the same way, using (A1), (A2) and the equation of $i(\pi) = i_{L0}$, the α can be calculated as the equation (A3).

$$i(\pi) = \frac{Vin-nV_{out}}{wL}(\pi - \phi) + i_{L1} = i_{L0} \tag{A3}$$

Then, the equation of (A3) is arranged in α, voltage gain m, and phase-shift value of ϕ. And summarizing it as α,

$$\alpha = \frac{2\phi-(1-m)\pi}{m+2} \tag{A4}$$

The equation of (A4) is same with expression (8). By substituting α into equation of (A1) and (A2), then the equation of (6) and (7) can be derived.

B. Derivation of transferred power of the semi-DAB

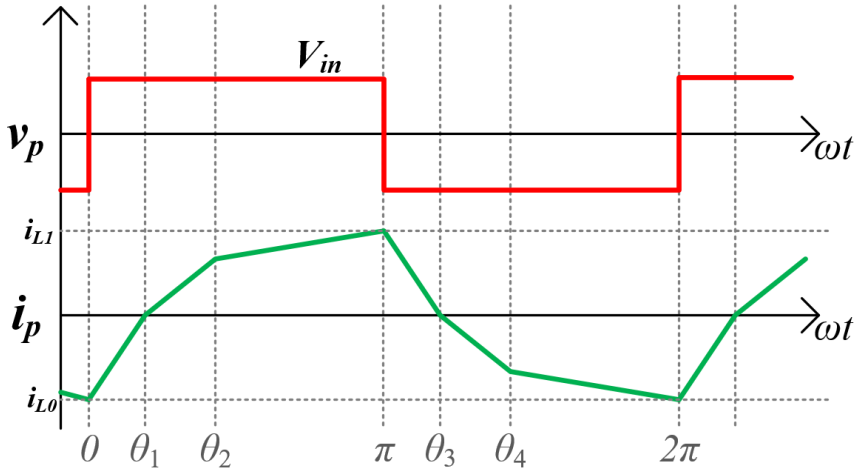

Fig. B1. The voltage and current waveform of semi-DAB converter

The Fig. B1 illustrates the voltage and current waveform of primary side for semi-DAB converter. Assuming as ideal semi-DAB converter, the input power is equal to the delivered output power, and the input power is derived as the equation of (9) and (10). Also due to the characteristics of semi-DAB, the half period is negative symmetric, so only the power up to 0 ~ π can be obtained. From 0 to π, the input voltage is V_{in}. And the average current can be calculated the area under the current waveform for 0 to π. The area under the current waveform 0 to π is can be calculated in equation (B1)

$$i_{area} = \frac{1}{2}[-i_{L0} \cdot \phi + (i_{L0} + i_{L1})(\pi - \phi + \alpha)] \quad \text{(B1)}$$

In the equation (B1), substitute i_{L0}, i_{L1}, and α of equation (6),(7), and (8). Then, the average current can be obtained in equation (B2)

$$i_{avg} = \frac{V_{in}}{wL}\frac{1}{(m+2)^2}[-2m(m^2+2m+2)\phi^2 + 2(m^3+3m+2)\pi\phi + m(1-m)(2m+1)\pi^2] \quad \text{(B2)}$$

Then, the transferred power can be obtained by product of (B1) and input voltage. The input voltage is V_{in}, and have to divide into π, because the average current has to divide into period according to average equation. So, the power of the semi-DAB can be obtained as below:

$$P = \frac{V_{in}}{2\pi}\frac{V_{in}}{wL}\frac{1}{(m+2)^2}[-2m(m^2+2m+2)\phi^2 + 2(m^3+3m+2)\pi\phi + m(1-m)(2m+1)\pi^2 \quad \text{(B3)}$$